Topaz, Stratus, Tropos, Garnet, and Duros PMC Graphics Boards User's Manual

Rastergraf

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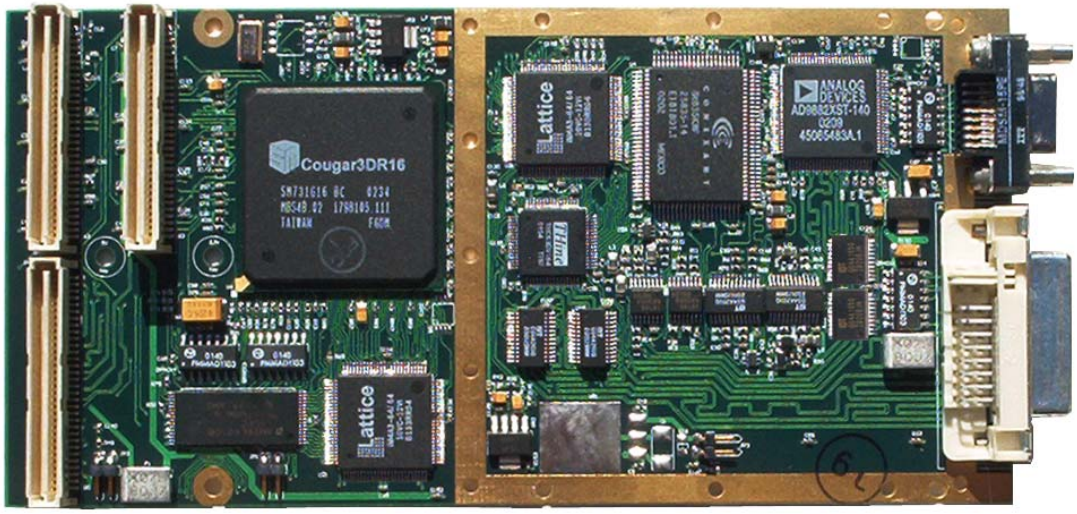

Introduction

This manual provides information about how to configure, install, and program the Rastergraf Silicon Motion SM731-based Topaz, Stratus, Tropos, Garnet, and Duros PMC graphics display controllers. When used with appropriate PMC-to-host adapters, PCI and CompactPCI compatible computers can also be supported.

This manual is broken down into six chapters:

Chapter 1: General Information
Chapter 2: Specifications
Chapter 3: Connector Pinouts and Cable Information
Chapter 4: Installing Your Graphics Board
Chapter 5: Programming Devices and Memories
Chapter 6: Troubleshooting

Chapters 1-3 provide background material about the graphics boards. Understanding the information in the chapters, however, is not essential for the hardware or software installation. If you want to perform the installation as quickly as possible, start with Chapter 4. If you have problems installing the hardware, refer to Chapter 6 for help.

Getting Help

This installation manual gives specific steps to take to install your Rastergraf board. There are, however, variables specific to your computer configuration and monitor that this manual cannot address. Normally, the default values given in this manual will work. If you have trouble installing or configuring your system, first read Chapter 6, "Troubleshooting". If this information does not enable you to solve your problems, do one of the following:

1) call Rastergraf technical support at: (541) 923-5530
2) send E-mail to: support@rastergraf.com .

If your problem is monitor related, Rastergraf technical support will need detailed information about your monitor.

Board Revisions

This manual applies to the following board revision levels:

Tropos/Stratus Fab Rev 1
Duros/Garnet Fab Rev 1
Topaz Fab Rev 0, 1, 2

Manual Revisions

Revision 3.1	April 2007	Rastergraf version
Revision 3.2	September 2007	Update RIO info
Revision 3.3	February 12, 2008	Fix part numbers, add LVDS info, change cable info.
Revision 3.4	December 6, 2013	Changes for Topaz Rev 1. Remove fax, update address, add RG-101 pinout
Revision 3.5	January 6, 2014	clean up some text in Ch. 3
Revision 3.6	February 7, 2017	clean up and correct tables in Section 3.20.
Revision 3.7	May 5, 2017	Changes for Topaz Rev 2. Moved jumpers, added option for VGA Ch 2 on Ch 1 on DVI-I

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The information in this document is subject to change without notice. The specifications of the graphics boards and other components described in this manual are subject to change without notice. Although it regrets them, Rastergraf, Inc. assumes no responsibility for any errors or omissions that may occur in this manual. Customers are advised to verify all information contained in this document

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Conventions Used In This Manual

The following list summarizes the conventions used throughout this manual.

`Code fragments`	Code fragments, file, directory or path names and user/computer dialogs in the manual are presented in the `courier` typeface.
Commands or **program names**	Commands, or the names of executable programs, except those in code fragments, are in bold.
System prompts and commands	Commands in code fragments are preceded by the system prompt, a percentage sign (%), the standard prompt in UNIX's C shell, or the hash mark (#), the standard UNIX prompt for the Super-User.
Keyboard usage	**<CR>** stands for the key on your keyboard labeled "RETURN" or "ENTER"

Note	Note boxes contain information either specific to one or more platforms, or interesting, background information that is not essential to the installation.

Caution	Caution boxes warn you about actions that can cause damage to your computer or its software.

Warning!	Warning! boxes warn you about actions that can cause bodily or emotional harm.

Chapter 1
General Information

1.1 Introduction

The Topaz, Stratus, Tropos, Garnet, and Duros comprise a set of closely related designs that have been tuned to address a variety of requirements.

Originally starting with the Stratus as the fully configured version and Tropos as the low parts count version, the line was expanded into the analogous Garnet and Duros which are rugged, conduction cooled versions adding 2 thermal layers and, on the Duros, the ability to produce STANAG 3350 A-C output modes.

The final iteration is the Topaz, a non-conduction cooled design, which is intended to subsume the Stratus and Tropos. It:

a) includes the new features added in the Garnet and Duros,

b) using an MDR26 connector, adds the optional capability to provide LVDS on the front panel,

c) replaces the Stratus front panel MDSM Video I/O connector with an MDR20 for easier cable construction,

d) adds a dual front panel VGA connector option,

e) adds the 3.3V local regulator option that was dropped on Garnet and Duros.

The following page shows a table of the features of the boards in a comparative format to ease understanding what each version provides. Following that are block diagrams of each board, and then some explanatory sections covering the board functions.

Table 1-1 Board Feature Summary

	Topaz	Stratus/ Garnet	Tropos/ Duros
Silicon Motion SM731 2D/3D engine with 16MB SDRAM	yes	yes	yes
1600x1200 single VGA	yes	yes	yes
1024x768 dual VGA	yes	yes	no
1280x1024 single/1024x768 dual LVDS	yes	yes	yes
1600x1200 single DVI	yes	yes	option
S-Video/NTSC/PAL/SECAM single output	yes	yes	Duros
Interlaced/non-interlaced, Sync-On-Green	yes	yes	Duros
STANAG 3350 A-C output option	yes	no	Duros
DVI Input mode	yes	yes	no
RGBHV, RGB, and STANAG Input modes	yes	yes	no
S-Video/NTSC/PAL/SECAM Input modes	yes	yes	no
Dual front panel VGA connector option	yes	no	no
Dual VGA via DVI b/o cable option	yes	Stratus	no
Dual VGA rear panel option	yes	yes	no
LVDS options – front/rear	yes	rear only	rear only
MDR26 LVDS front panel connector option	yes	n/a	n/a
Single DVI options – front/rear	yes	yes	yes
Composite/S-Video output	yes	yes	yes
MDSM-16 Video I/O connector	no	Stratus	no
MDR20 Video I/O connector	yes	no	no
2 Kb serial EEPROM and LM75 thermal sensor	yes	yes	yes
3.3V & 5V PCI Bus Signaling	yes	yes	yes
33/66 MHz PCI Bus Speed	yes	yes	yes
CCPMC form factor compatible	yes	yes	yes
Full CCPMC version with thermal layers	no	Garnet	Duros
Local 3.3V regulator	yes	Stratus	Tropos
Side 1 only component loading	yes	yes	yes
Field reprogrammable VGA BIOS	yes	yes	yes
SDL Graphics Subroutine Package	yes	yes	yes
SDL-based WindML and BIT	yes	yes	yes
Windows 2K/XP graphics drivers	yes	yes	yes
Windows 2K/XP video input drivers	yes	yes	no
Xfree86 Version 4.3 for Linux and VxWorks	yes	yes	yes
X video in extensions for Linux and VxWorks	yes	yes	no
RG-101 Rear I/O compatible version (PCB Rev 1)	yes	no	no

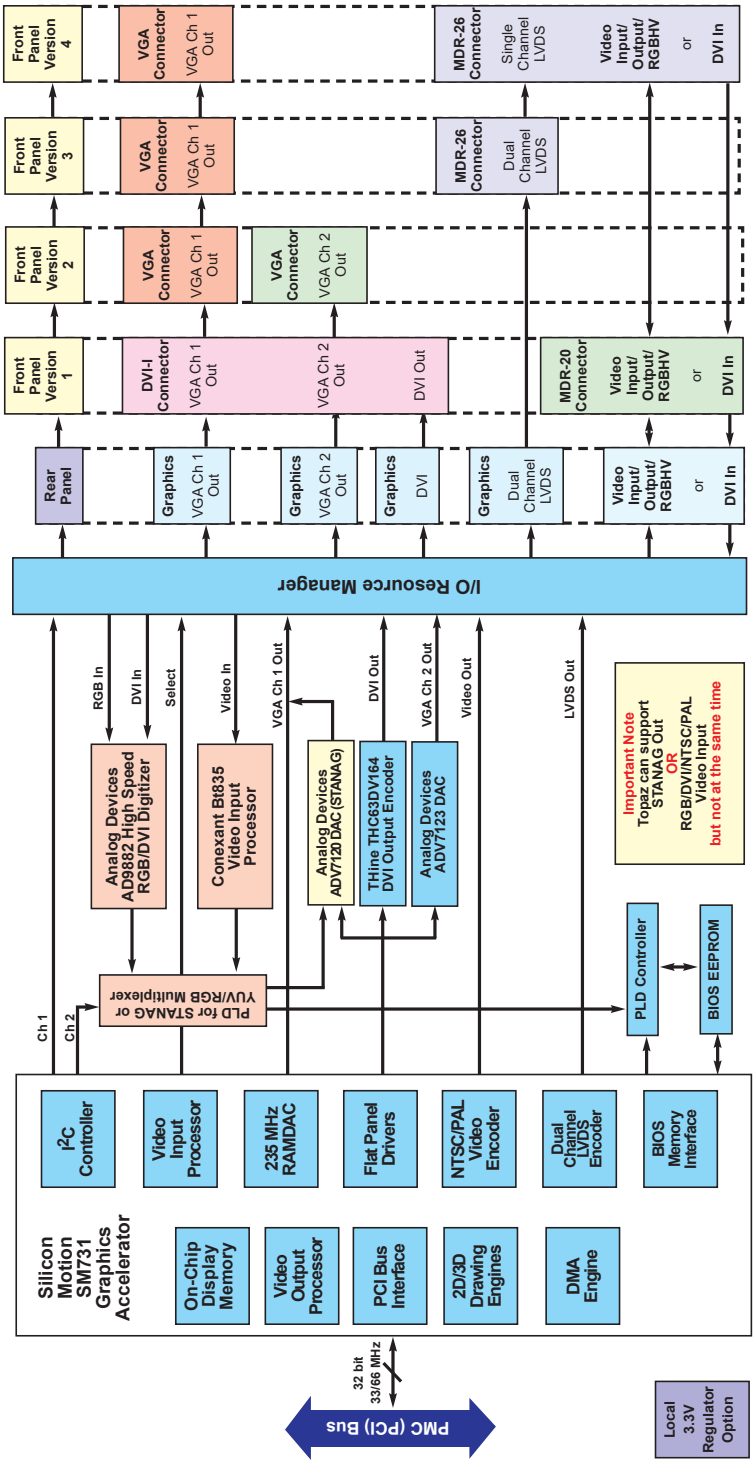


Figure 1-1 Topaz Block Diagram

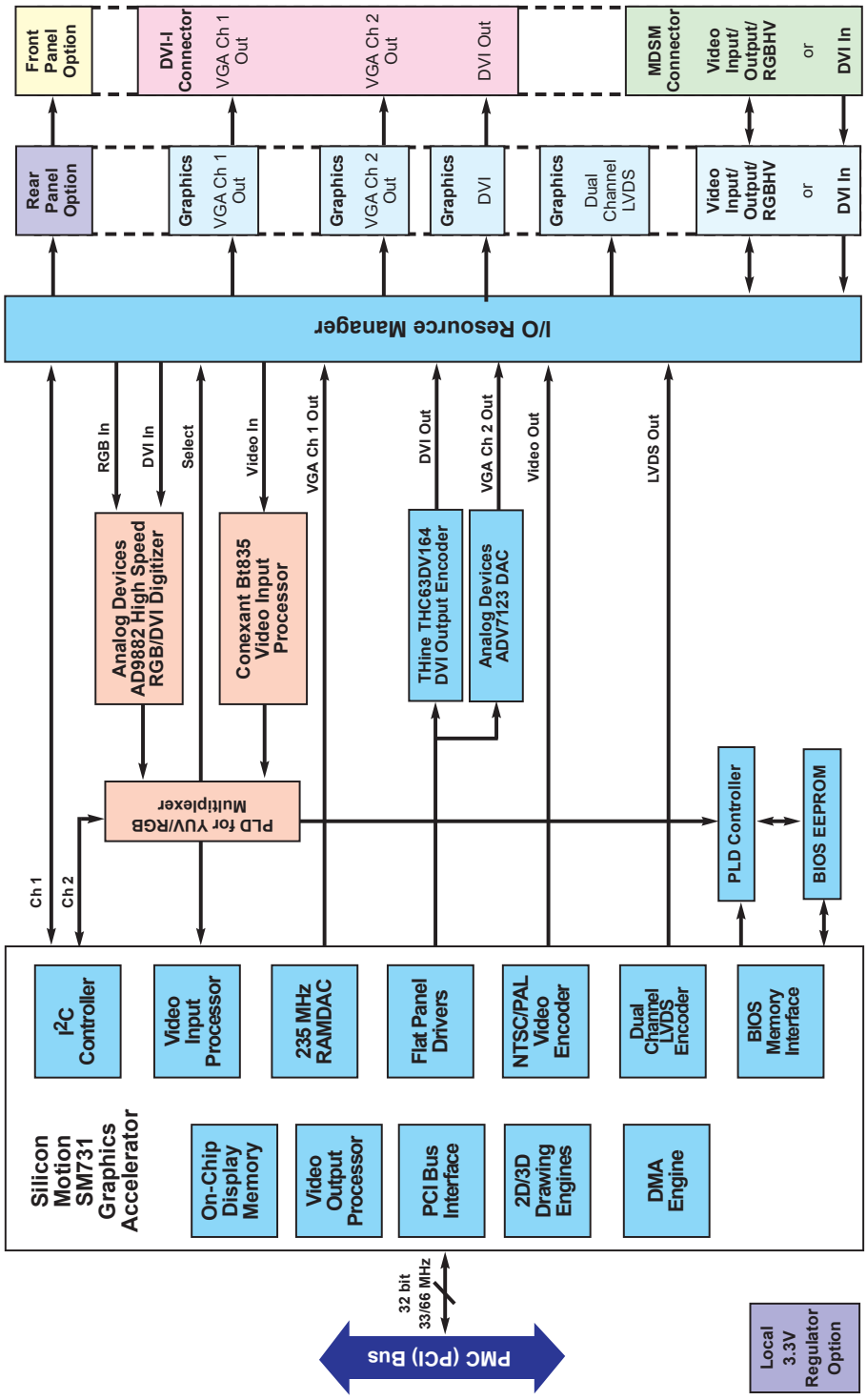


Figure 1-2 Stratus Block Diagram

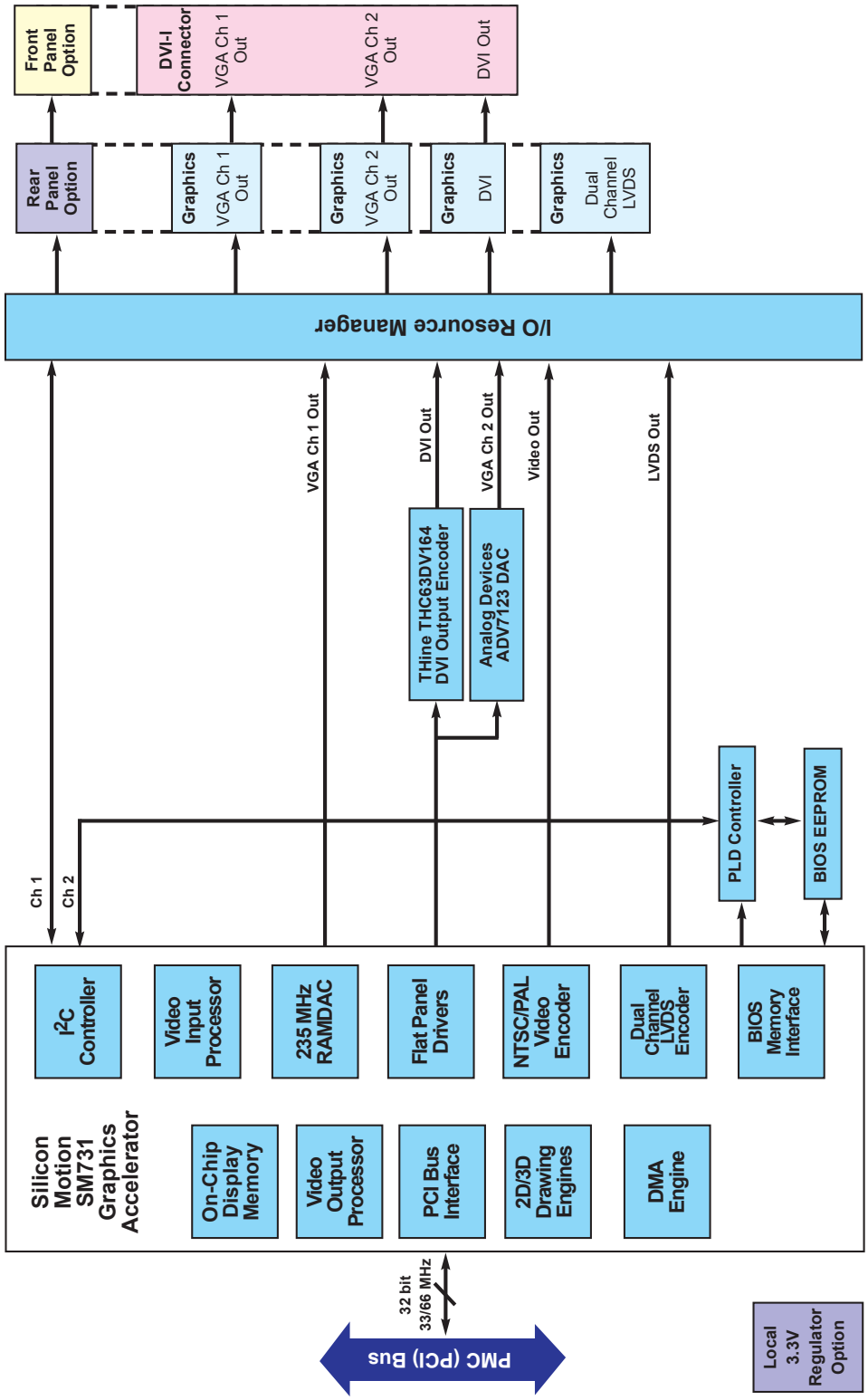


Figure 1-3 Tropos Block Diagram

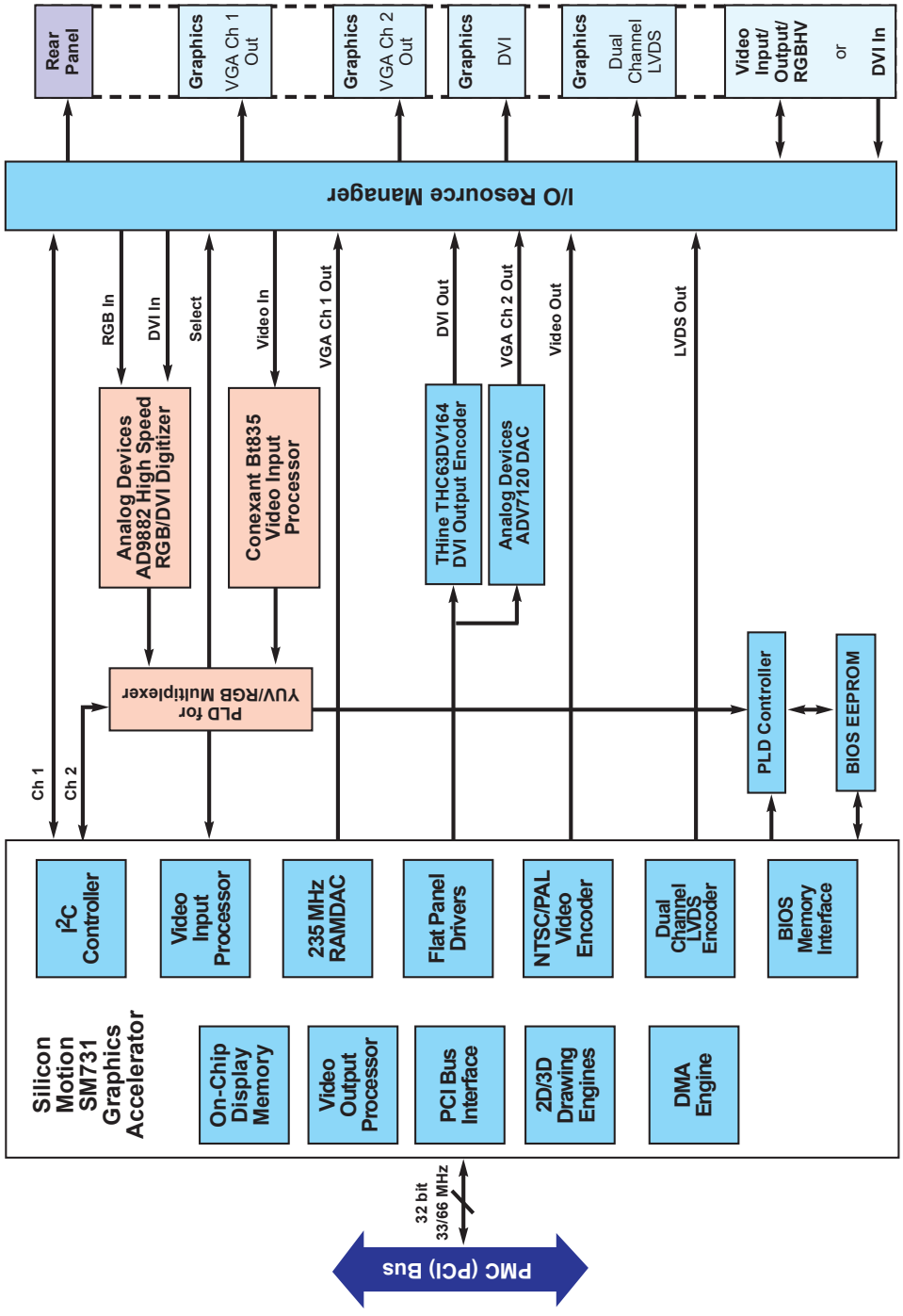


Figure 1-4 Garnet Block Diagram

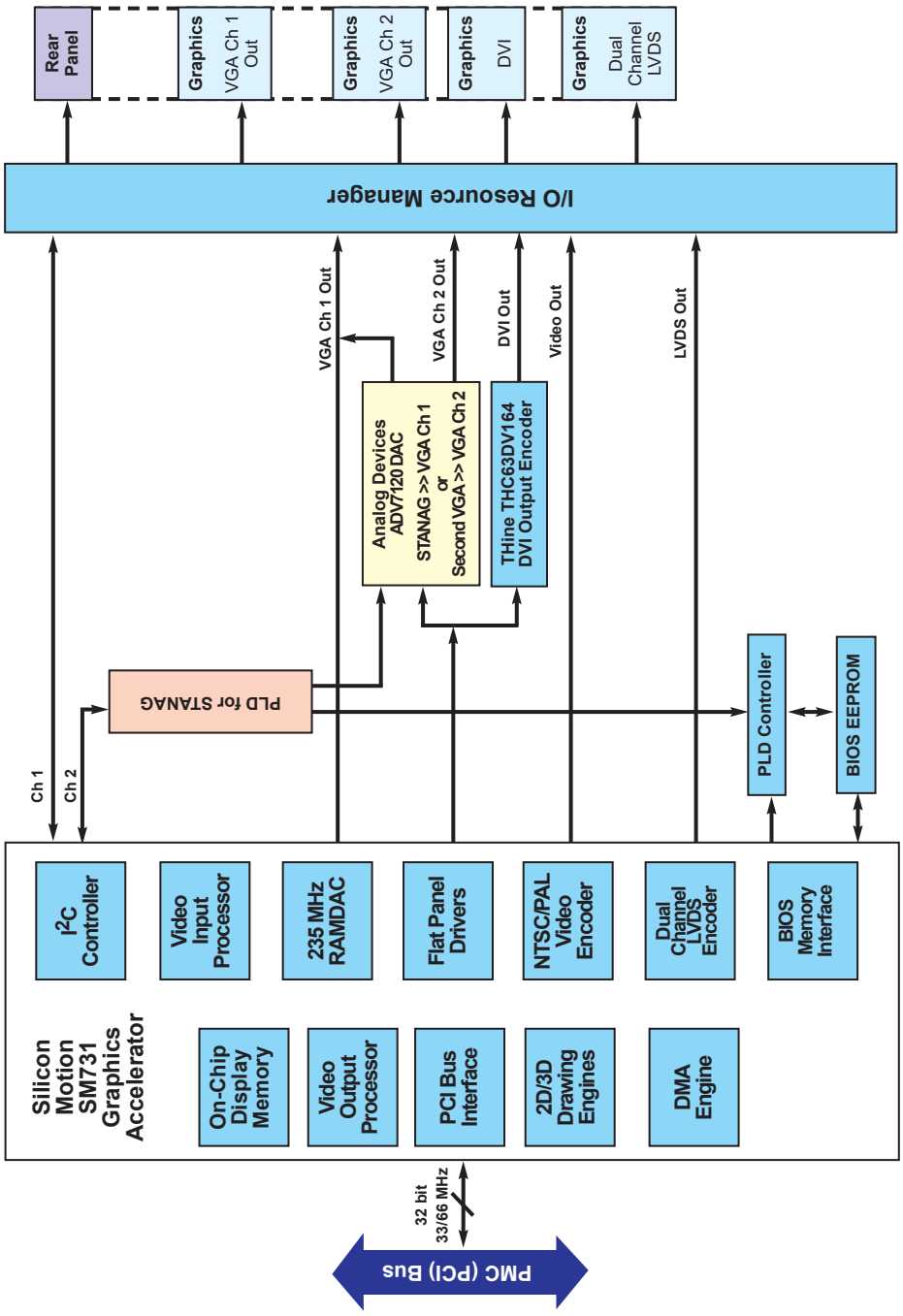


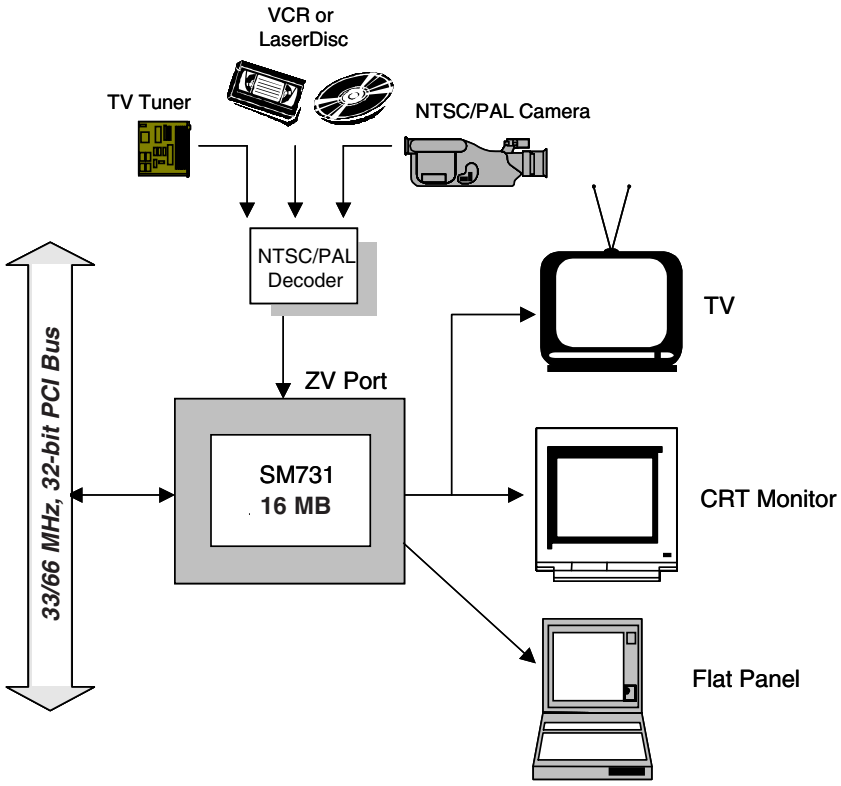
Figure 1-5 Duros Block Diagram

1.2 SM731 Graphics Controller

1.2.1 Overview

The SM731 is a low power 2D/3D display controller with 90, 180, and 270 degree hardware rotation. Silicon Motion's ReduceOn™ technology for the SM731 implements functions in hardware that were previously performed in software, allowing easier driver development. ReduceOn technology intelligently monitors the activity on the device and optimizes the power as necessary to maximize performance and power consumption. This level of power management is possible since each functional block and engine clock can be dynamically controlled to actively reduce the overall power consumption.

Figure 1-6 SM731 Application Block Diagram



1.2.2 Detailed Description

The SM731 delivers full-featured 3D, a unique memory architecture designed to enhance 3D/2D performance, enhanced multi-display capabilities, and Motion Compensation for DVD. Software support is available under Windows 2K/XP and Linux/XFree86.

A robust 128-bit Drawing Engine provides excellent 2D performance. The Drawing Engine supports 3 ROPs, BitBLT, transparent BLT, pattern BLT, color expansion, line draw and Alpha blending. The Host interface Unit allows support for PCI up to 66 MHz.

The SM731 incorporates an IEEE Floating Point Setup engine as well as a full-featured 3D rendering engine. The 3D engine pipeline was designed to operate in a balanced manner, allowing setup of 6 million triangles per second (125MHz core frequency) and rasterization of 125 Mpix/s. The dual pipe Texture engine can output 250 million Texels per second. Among other features, SM731 natively supports MIP mapping, Alpha blend, Specular highlights and Fog, Stencil planes, W buffer and fog, Bump Mapping, and Z engine.

The SM731 integrates 16 Mbytes of on-board SGRAM (SDR) over a 64-bit memory bus operating at up to 150 MHz. The 1.2 GB/sec peak bandwidth available allows concurrent support of large displays and other processing functions at optimum performance.

SM731 can drive two independent digital displays or simultaneously drive LCD, CRT and TV displays. It also incorporates two 112 MHz Max pix clock LVDS channels that can drive two separate panels or a single high-resolution panel (up to UXGA). Support for all ACPI power states is provided. A high quality TV encoder, VGA Core, LCD Backend Controller and 235 MHz RAMDAC are incorporated as well.

The SM731's Motion Compensation block, Video Processor block, and Video Capture Unit provide superior video quality for real-time video playback and capture. When combined with performance CPUs, the Motion Compensation block allows full frame playback of DVD video content without the need for additional hardware. The Video Processor supports multiple independent full screen, full motion video windows with overlay. Each motion video window uses hardware YUV-to-RGB conversion, scaling, and color interpolation. When combined with multi-view capabilities of the chip, these independent video streams can be output to each of two display devices and bilinear scaled to support applications such as full screen display of local and remote images.

1.2.3 SM731 Features

High Performance Hardware Graphics Support

- 128-bit single-cycle graphics engine
- 16MB on-chip frame buffer memory with 128-bit interface
- IEEE Floating point setup engine
- Bi-linear/Tri-linear filtering, MIP-mapping, vertex and global fog
- Multi-texture, bump mapping, texture compression
- Source/destination alpha blending, Specular highlights
- Z-buffering, dual-texture pipelines
- BitBLT, line draw, Polygon/rectangle fill
- Hardware cursor and pop-up icons

Analog RGB Display Support

- 640 x 480 to 1600 x 1200 non-interlaced at 8, 16 or 24 bits/pixel
- Integrated NTSC/PAL video formats
- Composite and S-Video (Y/C) signal interfaces

Panel Support

- Integrated Dual Channel LVDS transmitters with DualMon support
- QuickRotate feature for instantaneous rotation

On-Chip Dual Display Support

- RGB+VIDEO (NTSC/PAL). LVDS+RGB (VGA)
  LVDS+LVDS, and LVDS+VIDEO

Video Capture and Playback Support

- Zoom video port with live video display or single-frame capture
- Full-screen video or in a window with or without graphics overlay
- Video window may be of arbitrary size and on any pixel boundary
- Multiple independent hardware video windows
- Independent video capture and display subsystems
- Arbitrary XY scaling and up to 8x zoom on video input stream
- YUV capture data directly from host using on-chip DMA controller
- Motion compensation for full-speed DVD playback

PCI Bus

- 32-bit 33/66 MHz PCI 2.1 interface with burst-mode capability
- 264 Mbytes/sec peak data transfer rate at 66 MHz
- DMA bus-master capability
- Enhanced ReduceOn™ power management
- ACPI compliant

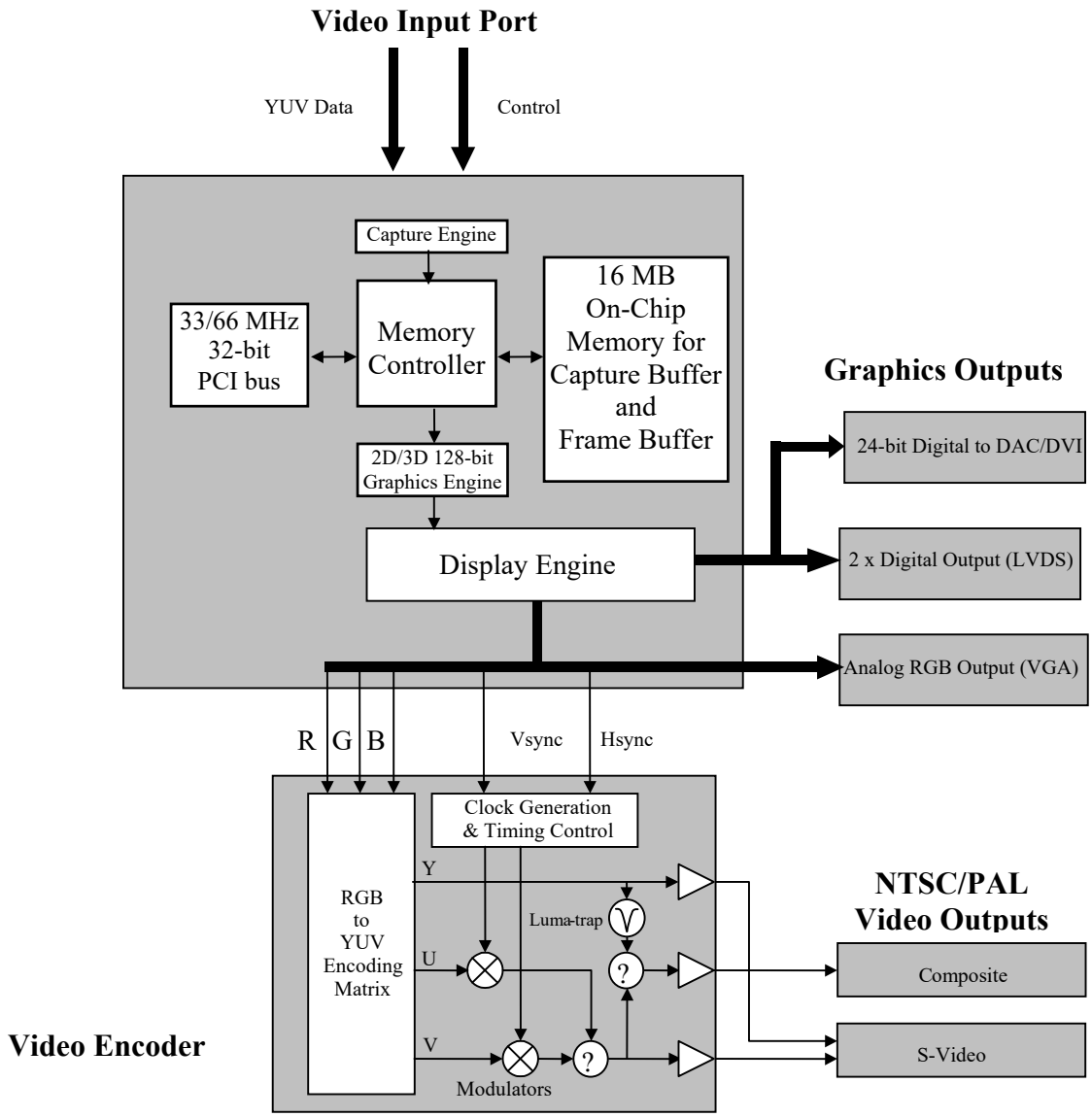


Figure 1-7 SM731 Detail Block Diagram

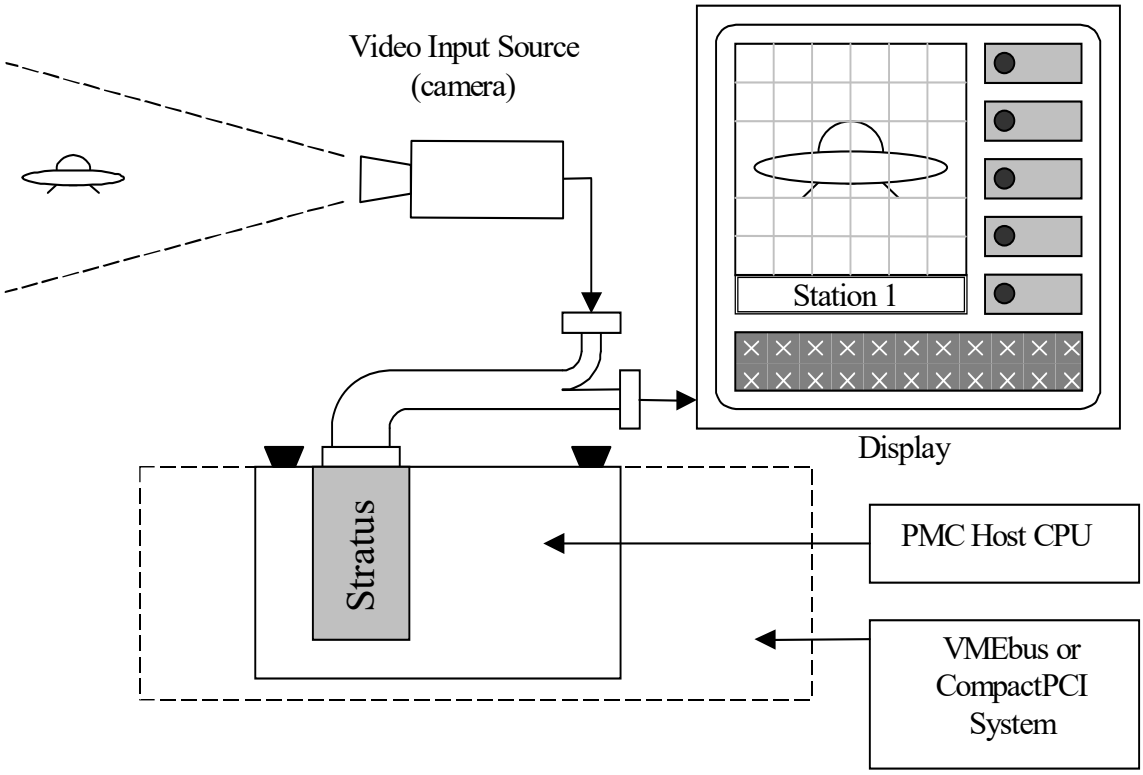
1.3 Video Capture and Playback

The Topaz, Stratus, and Garnet are ideal solutions for industrial graphics applications. They combine a powerful hardware graphics engine with support for multiple display devices including VGA, DVI, and LVDS displays, and NTSC/PAL video monitors.

They also provide video capture support from NTSC/PAL rate and RGBHV or DVI up to SXGA enabling real-time full-frame-rate display of live video as well as “frame-grabber” functionality that can upload images to the host.

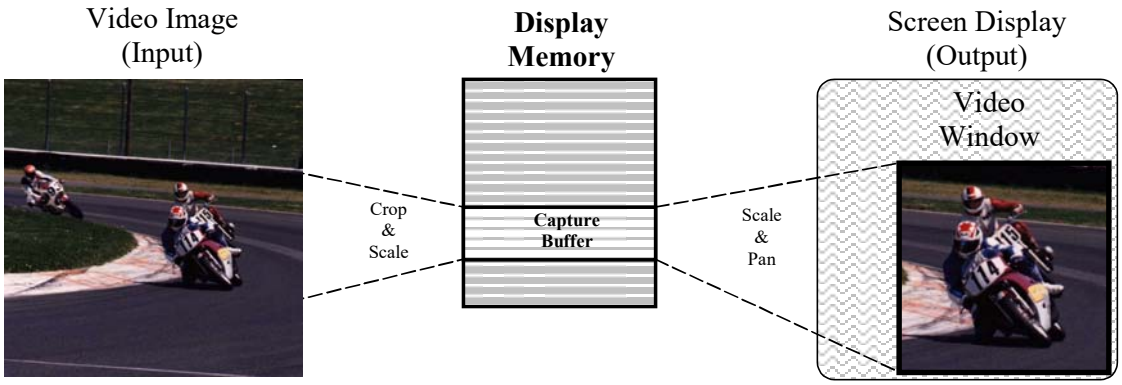
Video input may be easily included in a wide variety of applications. The use of video input can greatly benefit control and monitoring applications as a fundamental component of the user interface.

Figure 1-8 Video Capture and Playback Support



The display controller implements independent capture and playback subsystems. The capture system receives digitized video data through its 16 bit Video Input Port, which is driven by a multiplexer that selects between the on-board Bt835 NTSC/PAL video decoder (see Section 1.4) and the AD9882 RGBHV/DVI decoder (see Section 1.5). It places it in a capture buffer in display memory. The playback system retrieves the video data from the buffer and inserts it into a window in the display stream (screen image). The output display resolution and timing is not related to the incoming video resolution and timing so live interlaced video input may be incorporated into the graphics display without introducing video-related artifacts.

Figure 1-9 Capture Buffer and Display Memory



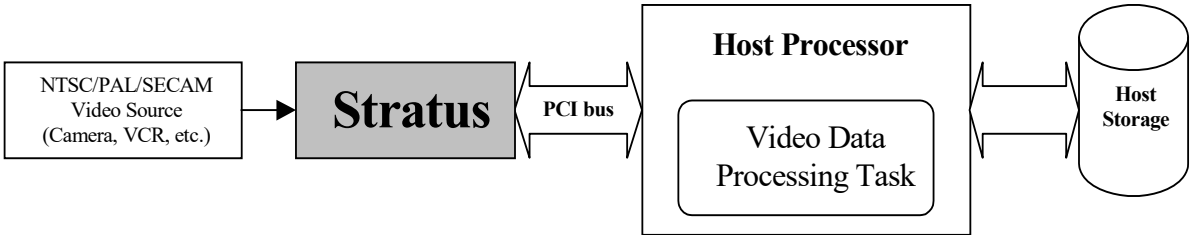
Video Playback

Once the incoming digitized video data has been placed into the capture buffer, the playback engine can retrieve it and incorporate it into the display output stream. The playback engine can up-scale (zoom) the contents of the video capture buffer before incorporating the capture image into the output stream. The image may either be made to fill the entire screen at the current resolution, or occupy a “window” within the larger output display. The window may be of arbitrary size and located on any pixel boundary. Color keying may be used to create non-rectangular windows, and/or to superimpose a graphics overlay on the video image.

Video Processing

Digitized video images in YUV format may be transferred from the capture buffer to host memory by the Topaz/Stratus/Garnet acting as a DMA PCI bus master. Once in host memory, the video data may be archived for retrieval and display at a later time. Alternatively, the host CPU can perform a color space transform on the YUV data or extract the luminance in order to generate an 8-bit gray-scale image. Image enhancement algorithms may be applied in surveillance or monitoring applications, or edge-detection algorithms in automated (robotic) process control applications.

Figure 1-10 Video Processing Data Path



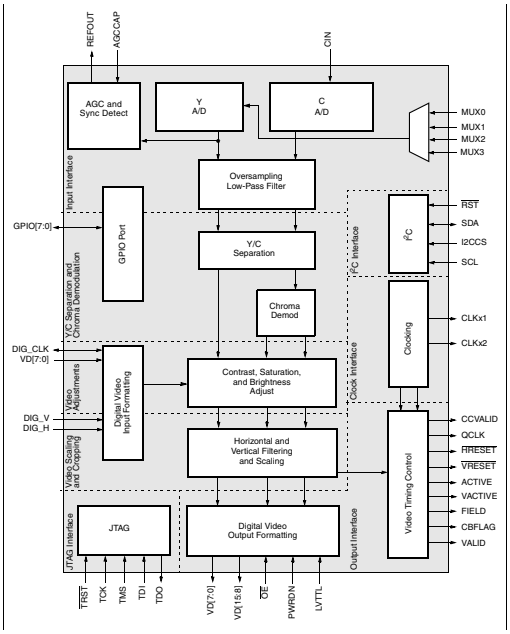
1.4 Bt835 NTSC/PAL/SECAM Digitizer

The Topaz/Stratus/Garnet provides a Conexant Bt835 video-capture processor, a single-chip decoding and filtered scaling solution for VCRs, cameras, and other sources of composite or component (S-Video or Y/C) video. It integrates video digitization, auto NTSC/PAL format detect and gain control, synchronization, 2H adaptive Y/C separation (comb filter), horizontal and vertical filtered down-scaling, user programmable peaking filter, and VBI data pass-through functions. An internal loopback can be enabled by software to connect the Composite Video Output to a Composite Video Input for testing

Using mixed signal and DSP circuitry, the Bt835 converts square pixel and CCIR601 resolution analog S-Video, NTSC, PAL, and SECAM base-band signals composite video into a scaled to YCrCb digital video stream

An input multiplexer allows the user to select between four composite input channels or an S-Video input. Hue, saturation, brightness and contrast controls provide added flexibility to enhance the appearance of the decoded image. Cropping and scaling can shrink the input image to no more than is needed for display. This reduces the bandwidth requirement of the capture and playback engines, leaving more time for graphics drawing and display refresh. A minimum scale factor of 0.071 allows a full-resolution video image to be reduced to icon size.

Figure 1-11 Bt835 Video Digitizer Block Diagram



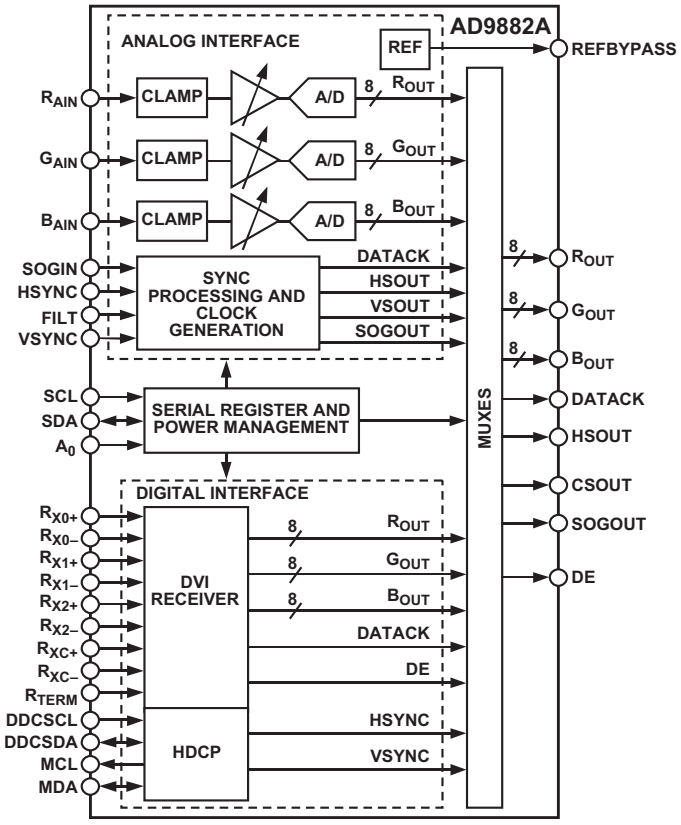
1.5 AD9882 RGBHV/DVI Digitizer

The AD9882 is a complete 8-bit 140 MSPS monolithic analog interface optimized for capturing RGB graphics signals. Its 140 MSPS encode rate capability and full-power analog bandwidth of 300 MHz supports resolutions up to SXGA (1280 x 1024 at 75 Hz).

The AD9882's on-chip PLL generates a pixel clock from HSYNC. Pixel clock output frequencies range from 12 to 140 MHz. PLL clock jitter is 500ps p-p typical at 140 MSPS. The AD9882 also offers full sync processing for composite sync and sync-on-green (SOG) applications.

The AD9882 also contains a DVI 1.0 compatible receiver and supports display resolutions up to SXGA (1280 x 1024 at 60 Hz). The receiver operates with true color (24 bit) panels and also features an intrapair skew tolerance of up to one full clock cycle.

Figure 1-12 AD9882 High Speed Digitizer Block Diagram

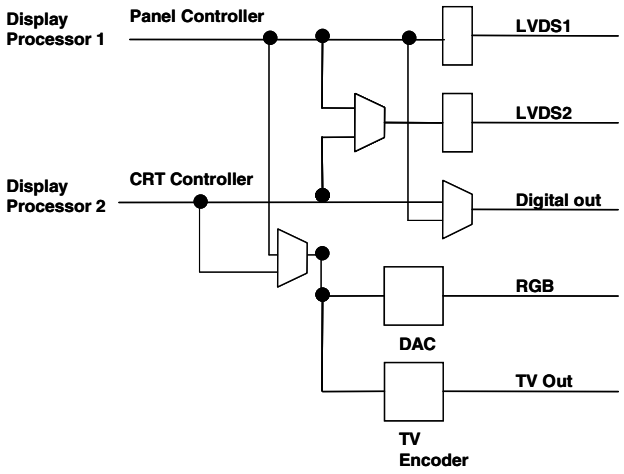


1.6 Flexible Display Support

The graphics boards support a variety of displays, including LVDS and DVI Flat Panels, Analog RGB (VGA) Monitors and Video Monitors. This enables it to be easily incorporated into a wide variety of applications. .

Although at a reduced display size, the graphics boards can drive two independent displays. One path is dedicated to RGB/DVI/LVDS displays and the other to RGB/TV/LVDS displays. Remember that performance will be compromised because there is only one drawing engine.

Figure 1-13 Display Channels



There are two independent display controllers inside SM731: The Panel Controller also referenced as the Primary Controller and the CRT Controller also referred to as the Secondary Controller. Because of this, SM731 is able to drive two screens with different images, from separate frame buffers and at independently programmable timing and resolution. Furthermore, the LCD panels can be programmed to display images from either controller, with some restrictions. The Digital Interface can drive data from either the Panel Controller or the CRT Controller, just like the LVDS2 interface. The LVDS1 interface is hardwired to drive data from the Panel Controller (primary display). If the digital interface (which goes to the external DVI encoder and the external Ch 2 VGA DAC) and LVDS2 interface are both turned on to drive the single pixel panels, their data source has to be the same either from the Panel controller or CRT controller. There will be no restriction if only one interface is on for single pixel panel or LVDS2 is used for double pixel panel.

See Section 5.2 for more information about the possible display combinations. There are several pages of diagrams that illustrate the amazing flexibility of the SM731 display modes.

1.6.1 TV Display

The Topaz/Stratus/Garnet supports base-band TV display output in either NTSC or PAL video formats. Both composite and S-Video (Y/C) are available.

The SM731 TV Encoder is somewhat limited in that it only allows 480 line output in NTSC mode. If your image is different from that, then you have to use the scaler to down- or up-size the image accordingly. Use of the scaler will affect the overall throughput of the chip and can limit the display size and video input pixel rates.

1.6.2 Analog RGB Displays

The boards are able to support display resolutions from 640 x 480 (VGA) up to 1600 x 1200 at up to 24 bpp. The Topaz/Stratus/Garnet can support a secondary VGA port, in which case both ports should be limited to 1024 x 768. The Secondary VGA output uses the spare pins on the DVI-I front panel connector or can be specified at order time to use the rear panel DVI output pins.

The secondary VGA DAC port is driven by the “Flat Panel” display controller section of the SM731. Displays ranging up to 1024 x 768 are practical when both channels are active. Some screen refresh-related artifacts may appear when a larger display format is used due to bandwidth limitations in the SM731.

1.6.3 STANAG 3350 A-C (Topaz/Duros)

STANAG Class A	875 Line, Interlaced
STANAG Class B	625 Line, Interlaced
STANAG Class B	525 Line, Interlaced

In the case of STANAG output, the video input multiplexer PLD is “stolen” in order to generate the special timing modes required for STANAG. For this reason, STANAG output automatically disables video input. In addition, the secondary VGA DAC is also “stolen”. It is wire-OR’d as an additional current source into the primary VGA output to generate the sync and blanking levels required by STANAG. Thus, you also lose the second VGA port. However, the STANAG implementation is extremely good, even including negative (below ground) sync. Properly programmed (using Rastergraf software) TopazPMC/1 and Duros boards are highly compliant to STANAG 3350 A-C in all aspects.

1.6.4 Flat Panel Displays

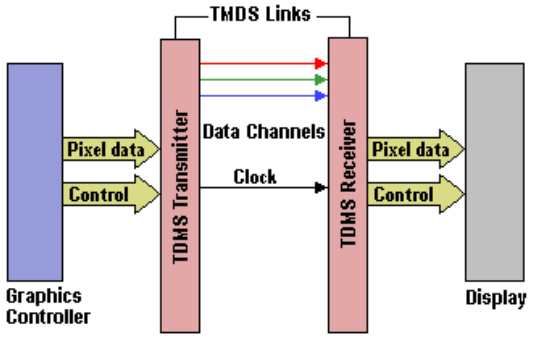
The graphics boards support 24-bit-per-pixel Flat Panel displays with either dual LVDS channels (1024 x 768 max) or using an external encoder connected to the Digital Out (see figure above), a single DVI channel (optional on Tropos and Duros). LVDS is available only via the PMC Pn4 rear panel I/O connector for all boards except Topaz, which has a front panel connector option as well.

1.6.4.1 DVI

The Topaz/Stratus/Garnet (optional on Tropos/Duros) is supplied with a DVI compliant transmitter. It provides high quality 24-bit true color digital output over twisted pair cables up to 3 meters in length. This length may be increased by using shielded twin-ax or fiber-optic cables. Displays ranging up to 1600 x 1200 are supported when best quality cables are used.

The DVI serializer is driven by the "Flat Panel" display controller section of the SM731. Three TMDS data channels send data at 1.65 Gbps per channel. Connections are made either through the front panel DVI-I connector or the rear panel I/O (PMC Pn4) as specified at order time.

Figure 1-14 DVI Flat Panel Output Block Diagram

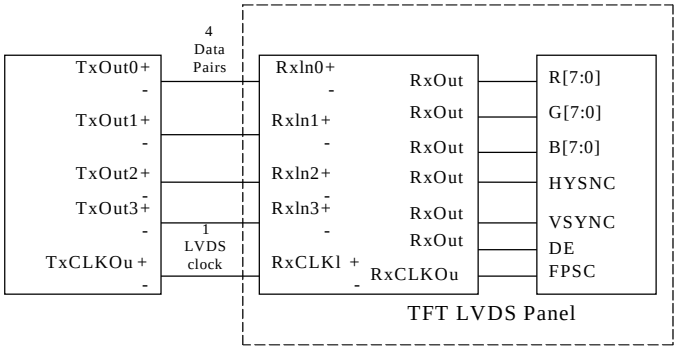


1.6.4.2 LVDS

The LVDS interfaces can be used to drive two independent panels, one displaying data from the Primary controller and the other displaying data from the Secondary controller. They can also be combined to drive a single, two pixels per clock, high-resolution panel. Each LVDS block compresses 24 bits of RGB data and 4 bits of LCD timing into four differential wire pairs, up to 392 MB per second at a maximum clock rate of 112 MHz. A fifth differential pair transmits the interface clock. This

way, each LVDS block can drive one SXGA+ panel (1400x1050x24 @60Hz). The LVDS1 Interface is hardwired to Panel Controller (Primary). It can be programmed to drive 18 or 24 bpp panels, and, if used in conjunction with the LVDS2 Interface, it can be used to drive a two channel, two pixels per clock panel of up to QXGA size (2048x1536).

Figure 1-15 LVDS Flat Panel Output Block Diagram



1.7 Front and Rear Panel I/O Options

The Topaz/Stratus/Garnet boards support front-panel I/O as well as rear-panel I/O via PMC Pn4. Not all hosts support rear-panel I/O. Those that do oftentimes have poorly routed traces from the PMC Pn4 connector to the host backplane connector, which makes them unsuitable for high frequency applications, especially LVDS and DVI. Check the host (carrier) documentation to determine what support is provided before considering rear panel I/O as an option.

Depending on the board, several input and output streams and connections are possible both to front panel connectors as well as the rear panel I/O (Pn4) connector.

Figure 1-16 Front and Rear Panel I/O Options for Topaz

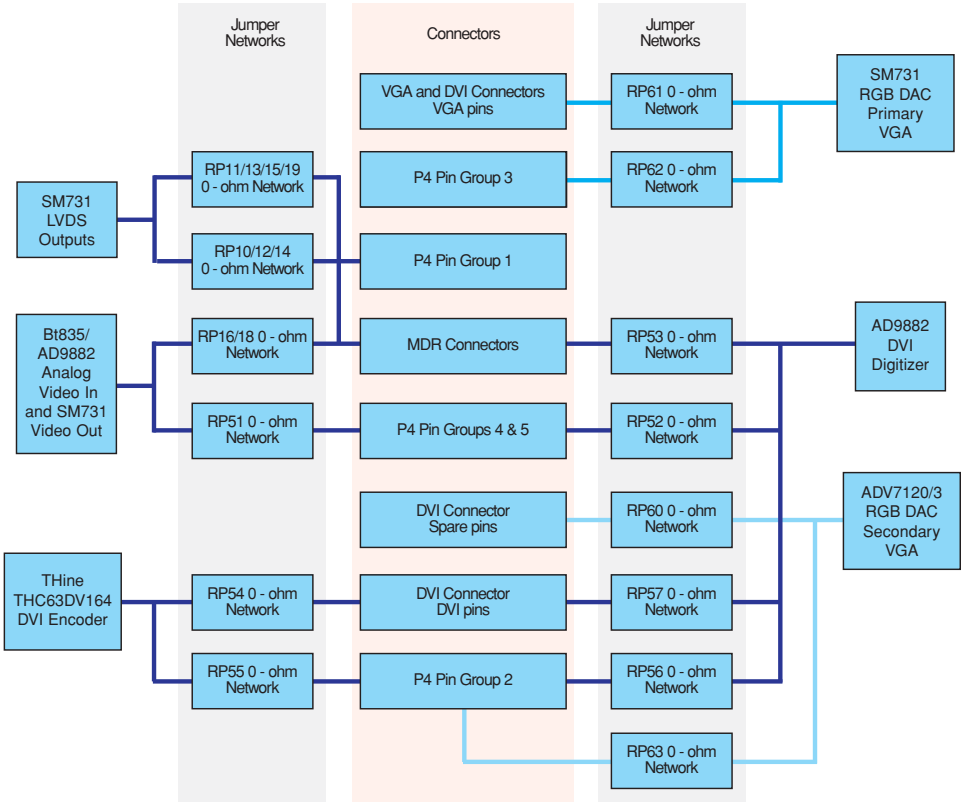


Figure 1-17 Front and Rear Panel I/O Options for Stratus

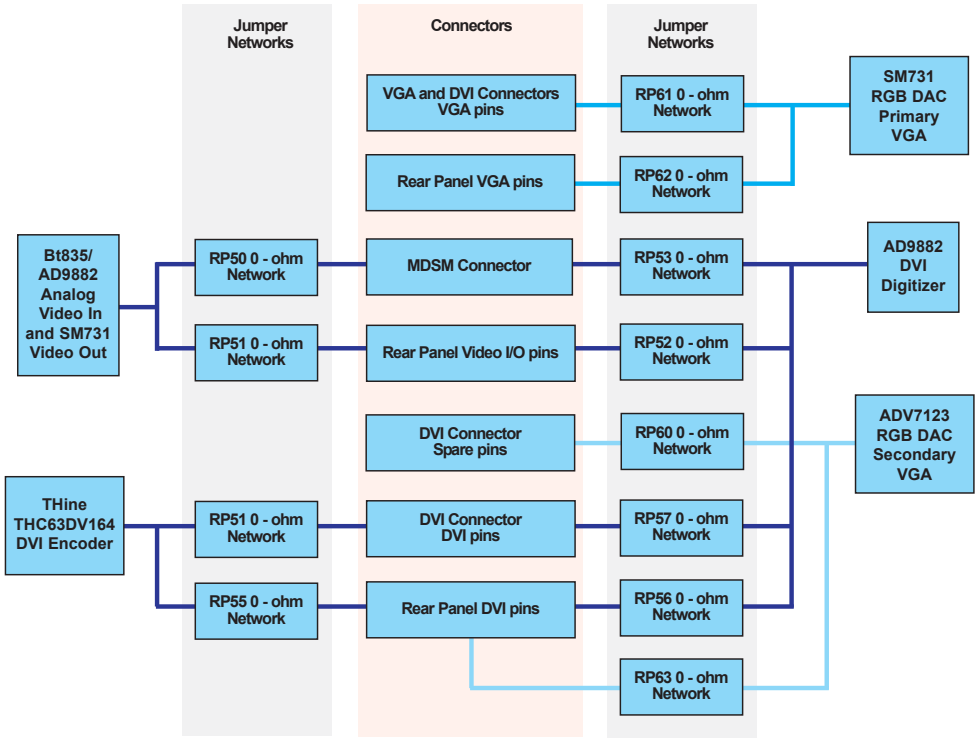


Figure 1-18 Front and Rear Panel Output Options for Tropos

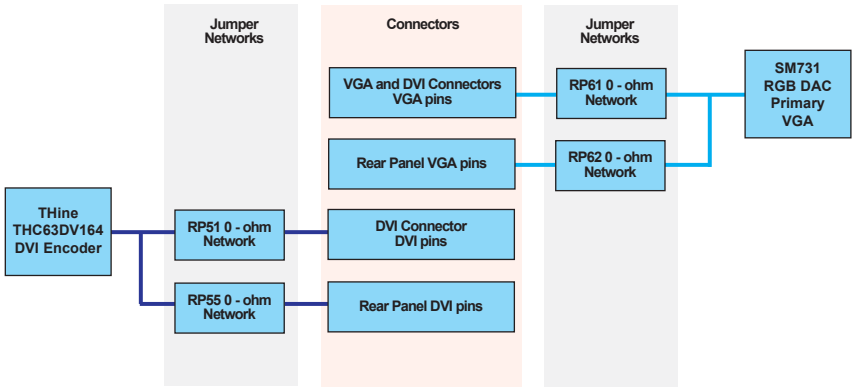


Figure 1-19 Rear Panel I/O Options for Garnet

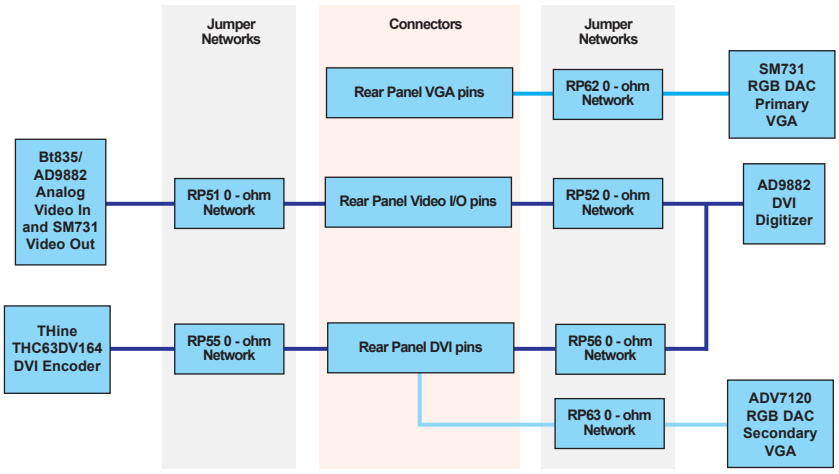
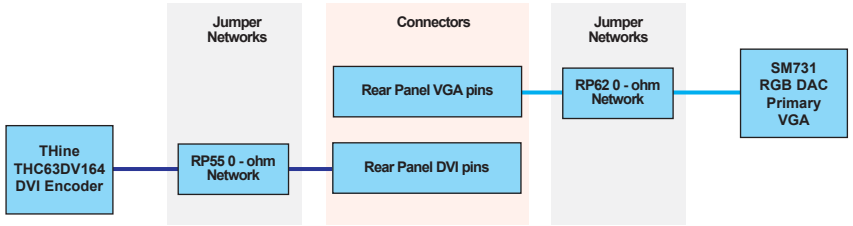


Figure 1-20 Rear Panel Output Options for Duros

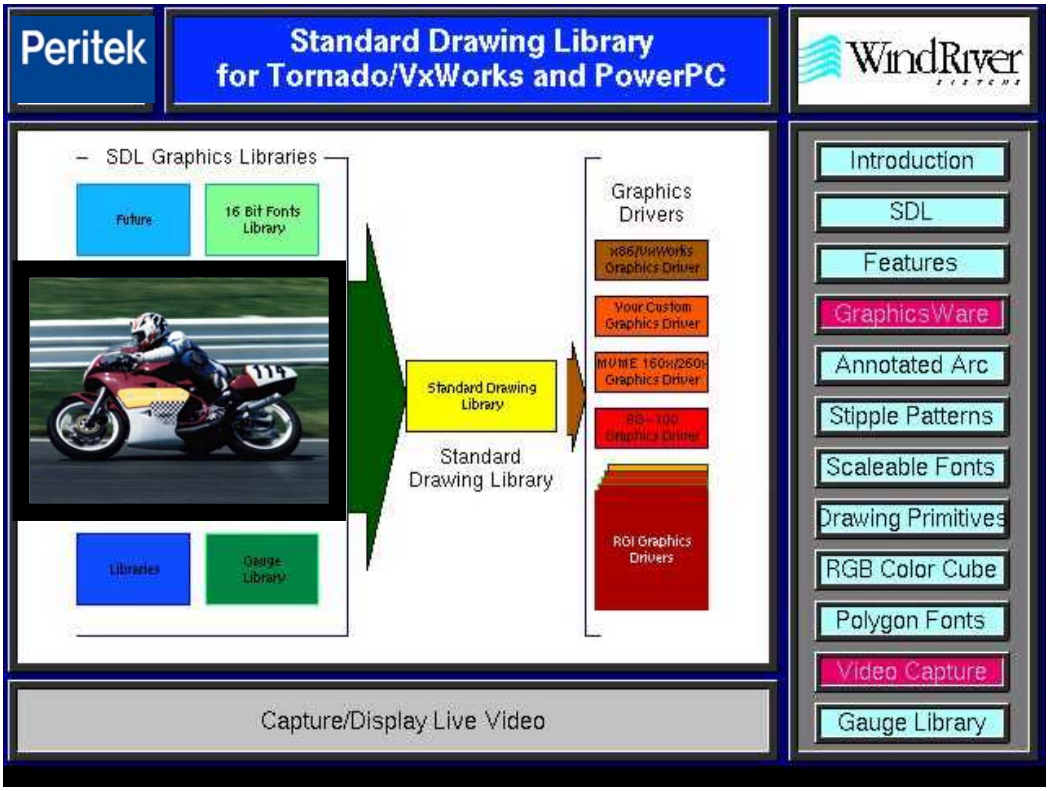


1.8 Software Support

Rastergraf software support is available for Linux, VxWorks, and Windows. Please consult Rastergraf for specifics, as all packages are not available on all systems. In general, we have:

- Windows 2K/XP Graphics Drivers with DirectX 8
- X Windows X11R6 (XFree86 Version 4.3) for Linux
- VGA BIOS
- SDL Graphics Subroutine Library for VxWorks and Linux
- VxWorks WindML (layered on top of SDL)
- Built-in Test (BIT) routines callable by CPU (layered on top of SDL)

1.9 Additional Details About SDL



SDL is a graphics library designed to be a device-independent programming interface. SDL is ideally suited to demanding board level and embedded systems applications. Drivers are available for selected host CPU boards and operating systems. SDL is supplied in object library format, which means that its target code size can be controlled by limiting the number of functions used in a given application. SDL has been

designed to run on any CPU and operating system that uses linear addressing and is supported by the GNU C compiler and linker. SDL is available in source for an additional cost – please contact Rastergraf sales.

SDL is easy to use. It includes a complete set of graphics primitives that interface to the SM731 graphics controller's accelerated functions. SDL also supports Stratus' video capture capabilities. All graphics primitives are drawn as single pixel lines. Rectangles, polygons, circles, ellipses, and chords can be filled with a solid color or stipple patterns.

Complete information about *SDL* is contained in the ***Standard Drawing Library* C Reference Manual** that is available for download from our web site at http://www.rastergraf.com.

SDL Feature Summary

- Solid (thin and wide) and dashed lines, polylines, and rectangles
- Pixblits to/from the display and host memory
- Filled and hollow polygons, ellipses, circles, sectors, and chords
- Solid and Pattern Fills – Pixel Processing
- Proportional and Fixed Width Fonts
- Clipping Rectangle and Logical Origin
- Video Capture Extensions

Table 1-2 SDL Functional Summary

Feature	Supported
VGA 640x480 to 1600x1200	Yes
8/16/24 bpp	Yes
DVI Output	Yes
Sync On Green	Yes
Video Capture - NTSC/PAL	Yes
Video Capture - (RGB) via AD9882	Yes
Video Capture - (mono) via AD9882	Yes
TV Out - NTSC/PAL	Yes
STANAG-A Timing	Yes

1.10 Additional References

Rastergraf documentation includes (hardware) User's Manuals and Standard Drawing Library (SDL) Manual. You can obtain some technical literature from the Rastergraf web page (http://www.rastergraf.com). Note that web links do change, so if the links given below are broken, just go the manufacturer's main web page and start your way in.

Silicon Motion SM731 Graphics Accelerator:

Contact Rastergraf (support@rastergraf.com)

Conexant Bt835 Audio/Video Decoder (now called CX25835):

http://www.conexant.com/products/entry.jsp?id=54

THine THC63DV164 DVIencoder:

Contact Rastergraf (support@rastergraf.com)

Analog Devices AD9882 RGB/YUV/DVI Digitizer and ADV7123 DAC:

AD9882: http://www.analog.com/en/prod/0,,765_806_AD9882A%2C00.html

ADV7123: http://www.analog.com/en/prod/0%2C2877%2CADV7123%2C00.html

1386-2001 and 1386.1-2001:
IEEE Standard for a Common Mezzanine Card Family: CMC and IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards

http://shop.ieee.org/ieeestore/Product.aspx?product_no=WE94922

The ***PCI Local Bus 2.3 Specification*:**

http://www.pcisig.com/specifications/conventional/conventional_pci_23/

Graphics Textbooks

Fundamentals of Interactive Computer Graphics
Addison Wesley, 1993. Foley and Van Dam

Principles of Interactive Computer Graphics
McGraw-Hill, 1979 Newman and Sproull

Chapter 2
Specifications

2.1 General

Graphics Processor:

Silicon Motion SM731 2D/3D High Performance 128-Bit Graphics Processors. Integrated on the same Multi-Chip Module (MCM) are the memory, LVDS encoders, and TV encoder.

The SM731 features an internal 235 MHz RAMDAC. It has a 256 entry Look Up Table (LUT), which is most commonly used for conversion of 8-bit pixels into full 24-bit RGB pixels. The RAMDAC has a programmable four-color bit-mapped 64 x 64 cursor. It supports VGA and common non-interlaced displays ranging from 640 x 480 up to better than 1600 x 1200. Signature registers enable display analysis for end-to-end testing.

The pixel size can be 8, 15, 16, or 24 bits. For 15 and 16 bpp, the pixel is divided into Red, Green, and Blue: 5:5:5 or 5:6:5. For 24 bpp, pixel is divided into Red, Green, and Blue and the data is ordered as packed pixels in memory.

Scroll, Pan, and Zoom:

Scroll - single line (smooth scroll).
Pan - anywhere on 16 byte boundaries
Zoom: horizontal: 2, 4, 8, 16, vertical: 2, 3 ,...,15, 16

Display Memory:

Display memory is 16 MB of 64-bits/word, byte addressable, no-wait state SDRAM provides eight pages of 1600 x 1200 using 8-bit pixels, four pages using 16-bit pixels, or two pages using 24 bpp packed pixel mode.

EEPROM Memory:

Flash EEPROM contains the VGA BIOS.

Digital Output: (Optional on Tropos)

Digital (DVI) output uses a THine (THC63DV164 DVI encoder connected to the SM731 flat panel output, which supplies 24-bit TTL level RGB plus HV. It samples and multiplexes the data and drives four differential pairs. Because of the high frequency nature of the TMDS signals, it is vital that matched length, shielded pair cable be used for DVI connections.

DVI-I Connector:	The DVI-I connector supplies both the digital DVI signals and dual analog VGA. Rastergraf can supply an adapter that allows a standard VGA cable to be connected to the DVI-I connector. A breakout cable can split out the DVI and the two VGA channels.
Composite Video Signal:	A jumper can be installed to select Sync-On-Green operation on boot-up. The signal has the following approximate values: 1 Volt peak to peak consisting of: 660 mV Reference White + 54 mV Reference Black + 286 mV Sync Level
Power-management:	With the proper software, the SM731 can power-down unused functions.
Fuse Element:	The +5V supplied to the front panel connectors is protected by a Positive Temperature Coefficient (PTC) resistor. It resets automatically when an overload is removed.
PCI Bus Access:	Programmable Bus Address Registers (BARs) in the SM731 map control and drawing engine registers, and display memory through its 33/66 MHz PCI interface.
PCI Bus Usage:	32-bit, 33/66 MHz, J1/J2/Pn4 Important Note: The SM731 at 66 MHz can be marginal. When using with the board at 66 MHZ on PMC-PCI or PCM-CompactPCI carrier, you ***MUST*** use an active version that has a local PCI-PCI bridge.
PCI bus Interrupts:	The SM731 can interrupt the PCI bus on the INTA line.
PCI Bus Master:	The SM731 can assume bus mastership of the PCI.
Bus Loading:	One PCI 2.1 compatible load
PCI Vendor ID:	Hardwired to 126Fh. Identify Silicon Motion as vendor.
PCI Device ID:	Hardwired to 0730h to identify the SM731 device. .
PCI Subsystem Vendor ID:	Powers up as 0x0000. Can be loaded by BIOS.
PCI Subsystem Device ID:	Powers up as 0x0000. Can be loaded by BIOS.

Power Requirements: All versions of ***REQUIRE***

+3.3V, +/- 5% @Current – please see below
+5V, +/- 5% @Current – please see below

A location for a local 3.3V regulator is provided on Topaz, Stratus, and Tropos for systems which do not supply it.

Power Measurements: The following power consumption figures have been measured with an effort to simulate worst case, with high-resolution displays and as much other simultaneous activity as possible. .

Testing Conditions: Windows 2000, dual display format is 1280 x 1024 x 32 bpp.

Cautionary Note: ***"Your mileage may vary".***

It would be prudent to add +10% for a maximum power estimate.

StratusPMC: Dual VGA out, capturing video

Also applicable to TopazPMC/2

Total power: 3.2W 5V, 0.25A
3.3V, 0.59A

GarnetPMC: Dual VGA out, capturing video

Total power: 3.17W 5V, 0.27A
3.3V, 0.55A

TroposPMC: Single VGA out

Also applicable to TopazPMC/1

Total power: 2.05W 5V, 0.02A
3.3V, 59A

DurosPMC: Dual VGA out

Total power: 2.6W 5V, 0.11A
3.3V, .62A

Environment:	Humidity:	5% to 90%, non-condensing
	Temperature:	-55 to +85 degrees C, storage
Topaz/Stratus/Tropos	Temperature:	0° to 70° C, operating
Garnet/Duros	Temperature:	-40° to 85° C, operating

IMPORTANT: GOOD AIRFLOW IS REQUIRED.

You should be able to measure at least 100 Linear Feet per Minute (LFM) at the board if you want to operate at the upper temperature limits. You can usually get this much air by using a 35 CFM-rated fan.

Please review the following pages for more information about the boards' requirements in particular and some general cooling and fan information.

PMC Compatibility: Complies with IEEE 1386-2001. Garnet and Duros also comply with VITA-20.

Module Size: IEEE 1386-2001 compatible, 149 mm x 74 mm

CCPMC Form Factor: The Topaz, Stratus, and Tropos boards are laid out to be Conduction Cooled PMC (CCPMC) form factor compatible. This is primarily intended to allow the boards to be used in applications that might require a display board for debugging purposes in system development.

The Garnet and Duros are ruggedized versions of Stratus and Tropos and should be specified for real CCPMC applications. The specifications are nearly identical, the main differences being that that there is no 3.3V regulator option on Garnet and Duros, and STANAG is supported on Duros but not on Tropos. STANAG is supported on Topaz, so there is a front panel, benign version available.

Front and Rear Access: As mentioned elsewhere, the Topaz/Stratus/Garnet are intended primarily for front panel use. However, most features are accessible on the PMC Pn4 rear access and the boards are available configured for this use.

If one were to choose rear panel I/O configuration, the Topaz/Stratus/Garnet can be supplied with no front panel connectors. In this case, only the connector grounds are still connected to circuit ground. All other connections are open.

The Garnet and Duros are full CCPMC versions and as such are available ONLY with rear panel access.

Care must be exercised in the use of rear panel, especially with LVDS and DVI, which require matched length pairs and signal impedance of 50 ohms differential. Most carrier and CPU boards were not designed for use with these graphics boards and will therefore not take into account these special needs. Please contact Rastergraf for assistance before committing to a rear panel access system design.

Note that as of the time of writing, there are no rear panel cables, PIM adapters, PMC carriers, or any other hardware aids available from Rastergraf that might be used as part of a rear panel system integration effort.

Ruggedization Option:

Rastergraf is not in the militarized business, but it does offer ”ruggedized” versions, which are the Garnet and Duros.

As compared to a full ruggedized products supplied by such companies as CWCEC and GE Fanuc which use mil-grade components and provide full component level traceability, Rastergraf board designs use standard distribution grade ***derated commercial temperature range or industrial temperature range components . No formal component tracking is maintained.***

The board is protected with a conformal coating. It is Miller Stephenson MS-460A spray-on, and is MIL-I-46058C, Type SR and MIL-T-152B compliant. The board is tested under extended temperature conditions:

Temperature: -40 to +85º C, operating
-55 to +125º C, storage

Ruggedization Levels: The following table shows the standard ruggedization levels. At the time of writing, complete shock and vibration testing has not been performed, but some boards have been tested enough to expect full acceptance is possible. Please contact Rastergraf Sales if you need this information.

Table 2-1 Rastergraf Ruggedization Levels Chart

Spec	Air-Cooled Level 0	Air-Cooled Level 50	Air-Cooled Level 100	Air-Cooled Level 200	Conduction-cooled Level 100	Conduction-cooled Level 200
Applicable Graphics Board(s)	Argus Gemini Sirena Eclipse3 Topaz Garnet	Gemini Sirena Eclipse3 Topaz Garnet	Gemini Sirena Eclipse3 Topaz Garnet	Eclipse3 Topaz Garnet	Garnet	Garnet
Operating Temperature (4, 6)	0°C to 50°C	-20°C to 65°C	-40°C to 71°C	-40°C to 85°C	-40°C to 71°C	-40°C to 85°C
Storage	-40°C to 85°C	-40°C to 85°C	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C
Humidity Operating	0 to 95% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing
Humidity Storage	0 to 95% condensing	0 to 100% condensing	0 to 100% condensing	0 to 100% condensing	0 to 100% condensing	0 to 100% condensing
Vibration Sine (1)	2 g peak 15-2 kHz	2 g peak 15-2 kHz	10 g peak 15-2 kHz	10 g peak 15-2 kHz	10 g peak 15-2 kHz	10 g peak 15-2 kHz
Vibration Random (2)	0.01 g2/Hz 15-2 kHz	0.02 g2/Hz 15-2 kHz	0.04 g2/Hz 15-2 kHz	0.04 g2/Hz 15-2 kHz	0.1 g2/Hz 15-2 kHz	0.1 g2/Hz 15 Hz-2 kHz
Shock (3)	20 g peak	20 g peak	30 g peak	30 g peak	40 g peak	40 g peak
Conformal Coat (5)	optional	optional	optional	optional	yes	yes
Order Option (7)	/CA or /CS	/A5A or /A5S	/A1A or /A1S	/A2A or /A2S	/C1A or /C1S	/C2A or /C2S

Notes:

1. Sine vibration based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 15 to 44 Hz, depending on specific test equipment. Shock and Vibration values not completely verified.
2. Random vibration 60 minutes per axis, in each of three mutually perpendicular axes.
3. Three hits in each axis, both directions, 1/2 sine and saw tooth. Total 36 hits.
4. Standard air-flow is 8 cfm at sea level. Some higher-powered products may require additional airflow. Consult the factory for details.
5. Conformal coating type to be specified by customer. Consult the factory for details.
6. Temperature is measured at the card interior (not at edge).
7. Last letter in ordering option: A for Acrylic Conformal Coating, S for Silicone Conformal Coating

2.2 Specifications Unique to Topaz, Stratus, and Garnet

Enhanced Functionality: The Topaz, Stratus, Garnet are the fully loaded versions. They add a Conexant Bt835 NTSC/PAL/SECAM video digitizer, Analog Devices AD9882 high-speed RGB/YUV/DVI digitizer, Analog Devices ADV7120 or ADV7123 VGA DAC, THine THC63DV164 DVI encoder, configuration EEPROM, and an LM75 thermal sensor.

Front Panel LVDS: The Topaz (only) can be ordered with Front Panel LVDS. It uses an MDR26 connector and follows the CameraLink (frame grabber side) pinout to make it easy to find cables. Please see Chapter 3 for pinout information.

VGA DAC and DVI Out: The versatile 24-bit flat panel (FP) port of the SM731 drives both an Analog Devices ADV7120 (Topaz, Stratus) or ADV7123 (Garnet) VGA DAC and a THine THC63DV164 DVI encoder. Thus, depending on the user requirements, the FP port can either supply a DVI encoded single channel graphics out or the second VGA port.

When used in the secondary port mode, display resolution is limited to about 1280 x 1024 because the SM731 can't supply pixels fast enough to do more. The DAC can support RGBHV or RGB with SOG. Properly programmed, interlaced is supported.

When used to supply DVI, the port can go up to 1600 x 1200. Best results are had when the pixel clock is limited to 150 MHz. Reduced blanking interval timing will further improve margins.

NTSC/PAL Digitizer: The Topaz, Stratus, and Garnet have a Conexant Bt835 Video Digitizer chip. It captures NTSC/PAL/SECAM composite video or S-Video with resolutions up to 768x576. It performs on-the-fly image scaling and clipping. The Bt835 has a multiplexer that can select composite and S-Video (separate chrominance and luminance). ***Note: All inputs have low pass filters.*** .

High Speed Digitizer:

The Topaz, Stratus, and Garnet have an Analog Devices AD9882 high speed RGB/YUV/DVI digitizer chip. It can capture analog RGBHV, RGB with SOG, or YUV (4:2:2). Or, when configured (by the factory) the AD9882 can capture DVI from the MDR20 (Topaz), MDSM (Stratus), or DVI (but then no longer out) pins.

The AD9882 is connected to the 16-bit SM731 video input port via a PLD which rearranges the data bits according to data type. When supplying RGB (or RGB encoded DVI) the normally 24-bit RGB [8:8:8] component is reduced to [5:6:5]. In YUV, the full 16-bit YUV is transmitted. When acquiring YUV (4:2:2), the luminance component can be forced to 0x80, yielding monochrome.

Analog Interface
140 MSPS Maximum Conversion Rate
Programmable Analog Bandwidth
0.5 V to 1.0 V Analog Input Range
500 ps p-p PLL Clock Jitter at 140 MSPS
3.3 V Power Supply
Full Sync Processing
Midscale Clamping
4:2:2 Output Format Mode

Digital Interface
DVI 1.0 Compatible Interface
112 MHz Operation
High Skew Tolerance of 1Full Input Clock
Sync Detect for “Hot Plugging”.

I^2C Channels:

I^2C is a simple low-speed 2 wire serial bus that is used to control a variety of on-board devices. The SM731 supports two I^2C ports.

The Primary port is connected to the VGA and DVI connectors and is used for DDC2B display monitor controls.

The Secondary port is connected to the THC63DV164 DVI transmitter, LM75 thermal sensor, AT24C02 2 Kb serial EEPROM, Bt835, and local control PLD.

2.3 Display Timing

The SM731 chip display timing is programmable. The following tables provide the timing values provided by Rastergraf software. Please note that the timing parameters vary by application.

Table 2-2 BIOS Display Timing Specifications

Active Display	Format	Bits per Pixel	Vertical Refresh	Horizontal Refresh	Pixel Clock
640 x 400	VGA	8	60 Hz	31.55 kHz	27 MHz

Table 2-3 VGA/Windows Platform Display Timing Specifications

Active Display	VESA Format	Bits per Pixel	Vertical Refresh	Horizontal Refresh	Pixel Clock
640 x 480	n/a VGA VGA VGA	8, 16, 32	60 Hz 72 Hz 75 Hz 85 Hz	31.5 kHz 37.9 kHz 37.5 kHz 43.4 kHz	25.175 MHz 31.5 MHz 31.5 MHz 36 MHz
800 x 600	SVGA	8, 16, 32	60 Hz 72 Hz 75 Hz 85 Hz	37.9 kHz 48.1 kHz 46.9 kHz 53.7 kHz	40 MHz 50 MHz 49.5 MHz 56.25 MHz
1024 x 768	UVGA	8, 16, 32	60 Hz 70 Hz 75 Hz 85 Hz	48.4 kHz 56.5 kHz 60.0 kHz 68.7 kHz	65 MHz 75 MHz 78.75 MHz 94.5 MHz
1280 x 1024	SXGA	8, 16, 32	60 Hz 75 Hz 85 Hz	64 kHz 80 kHz 91.1 kHz	108 MHz 135 MHz 157.5 MHz
1600 x 1200	UXGA	8, 16, 24	60 Hz 70 Hz 75 Hz 85 Hz	75 kHz 87.5 kHz 93.8 kHz 106.3 kHz	162 MHz 189 MHz 202.5 MHz 229.5 MHz

Table 2-4 SDL Platform Display Timing Specifications

Active Display	Analog/ DVI	Format	Bits per Pixel	Vertical Refresh	Horizontal Refresh	Pixel Clock
640 x 480	Both	VGA	8, 16, 32	75 Hz	37.65 kHz	30.72 MHz
800 x 600	Both	SVGA	8, 16, 32	75 Hz	47.03 kHz	48.90 MHz
1024 x 768	Both	UVGA	8, 16, 32	75 Hz	60.15 kHz	81.80 MHz
1152 x 900	Analog	Sun	8, 16, 32	72 Hz	67.54 kHz	103.74 MHz
1280 x 1024	Both	SXGA	8, 16, 32	75 Hz	80.17 kHz	138.54 MHz
1600 x 1200	Analog	UXGA	8, 16, 24	75 Hz	93.98 kHz	204.49 MHz

2.4 Monitor Requirements

Rastergraf boards can be used with a variety of monitors. For best performance a monitor should have the following features:

- VGA compatible 5 Wire RGB with separate TTL horizontal and vertical sync or 3 Wire RGB with sync on green (see note below)
- Switchable Termination (for monitor loopthrough)
- Height, pincushion, width, phase, and position controls
- Autotracking horizontal and vertical synchronization
- High bandwidth: 135 MHz at 1280 x 1024
  180 MHz at 1600 x 1200
- Horizontal refresh rate: 70 kHz at 1280 x 1024
  90 kHz at 1600 x 1200
- See Section 2.3 for complete display timing information

Notes

The software defaults to standard Multiscan 5-wire RGBHV (VGA compatible) settings. If you require Sync On Green, be sure to select **SYNC ON GREEN** when setting the Video Parameters.

Some versions of the graphics boards can support interlaced operation including STANAG A, B, and/or C. Please contact Rastergraf for more information.

Composite Video Signal: 1 Volt peak to peak consisting of:
660 mV Reference White +
54 mV Reference Black +
286 mV Sync Level

2.5 Verified Display and Capture Modes

The SM731 Graphics Controller is a flexible chip. It supports a single input capture channel as well as up to two independent outputs. It has widowing capabilities and a 128-bit high-performance drawing engine. But, the overall throughput is handicapped somewhat by a 64-bit memory bus. This section provides some tabulated information about the practical capabilities of the SM731. These sorts of limitations are common in graphics chips, but it's just unusual for a vendor to provide quantified data to the customers.

Note that this data is empirically obtained. There may be cases where a format that was observed to be clean might not be with high drawing engine activity. Special test software was used, not SDL or X Windows, in order to avoid application software dependencies.

2.5.1 Basic Format Evaluations

Notes:

nn-xx where nn = 640,1024,1280 or 1600 (nn = horizontal resolution)
xx = 8, 16, 24 or 32 (xx = bpp)
Resolutions tested: 640x480, 1024x768, 1280x1024, 600x1200
All modes use 60 Hz vertical refresh rate
Mode **FP** in VGA column means FP timing used for VGA out
Mode **VP** in DVI column means VP timing used for DVI out
-TV in VGA column means scaled TV out used instead of RGB out
Window is 640x488 YUV422; values are N (no), Y (Window only) or CAP (capture). **CAP** (capture) is 640x488 NTSC interlaced or 640x480 RGB @ 75Hz
Activity indicates display memory is under test to simulate application accesses
***streaks** : the DVI window is VERY sensitive to VGA timing, but the VGA window is NOT sensitive to the FP timing. ***streaks in window** : both capture windows displayed caused major streaking
***Max** : maximum vertical refresh rate before snow became apparent
***Max2** : same as *Max, but while capturing 1024x768@75Hz
"Max, Max2 is highest rate without snow or streaks, but capture update is slowed, which shows on moving video
Green Background means a clean format
Red Background means that a less than clean result was observed

In general, 16bpp mode has MUCH better performance than 32bpp mode. The DVI video window is very sensitive to the VGA refresh rate. If dual displays are required, one with a video window, performance is better if it is the VGA video window. Both displays can not use the same capture data for video window at higher resolutions - it gets ugly. The highest mode pair that would cleanly display both video windows was 1024x768x32bpp.

Table 2-5 Basic Display/Capture Format Capabilities

DVI mode	VGA mode	DVI Window	VGA Window	DVI Activity	VGA Activity	DVI Result	VGA Result	VFREQ *Max	VFREQ *Max2
1024-32	1024-32	N	N	Y	Y	OK	OK		
1024-32	1024-32	CAP	N	Y	Y	OK	OK	70	61
1024-32	1024-32	N	CAP	Y	Y	OK	OK	70	61
1024-32	1280-32	N	N	Y	Y	OK	OK		
1024-32	1280-32	CAP	N	Y	Y	light snow	snow		
1024-32	1280-32	N	CAP	Y	Y	light streaks	streaks		
1280-16	1280-16	CAP	CAP	Y	Y	light streaks	OK		
1280-16	1280-16	CAP	N	Y	Y	OK	OK	70	64
1280-16	1280-16	N	CAP	Y	Y	OK	OK	70	64
1280-16	1280-32	N	N	Y	Y	OK	OK		
1280-16	1280-32	CAP	N	Y	Y	light snow	light snow		
1280-16	1280-32	N	CAP	Y	Y	light snow	light snow		
1280-16	FP	CAP	N	Y	Y	OK	OK		75
1280-24	1280-24	N	N	Y	Y	OK	OK	65	
1280-24	1280-24	CAP	N	Y	N	OK	OK		
1280-24	1280-24	CAP	N	N	Y	light streaks	light streaks		
1280-24	1280-24	N	CAP	N	N	light snow	OK		
1280-24	1600-16	N	N	Y	Y	light snow	OK		
1280-32	1024-32	N	N	Y	Y	OK	OK		
1280-32	1024-32	N	N	Y	Y	OK	OKI		
1280-32	1024-32	CAP	N	Y	Y	snow	OK		
1280-32	1024-32	N	CAP	Y	Y	snow	OK		
1280-32	1280-16	N	N	Y	Y	OK	OK		
1280-32	1280-16	CAP	N	Y	Y	light snow	light snow		
1280-32	1280-16	N	CAP	Y	Y	light snow	light snow		
1280-32	1280-32	N	CAP	N	N	light snow	snow in window		
1280-32	1280-32	N	N	N	Y	light snow	OK		
1280-32	1280-32	N	N	Y	N	OK	OK		
1280-32	1280-32	N	Y	Y	Y	light snow	OK		
1280-32	1280-32	Y	N	N	N	*streaks	OK		
1280-32	1600-16	N	N	Y	Y	light snow	OK		
1280-32	FP	CAP	N	Y	Y	OK	OK	67	50
1600-16	1280-24-TV	N	N	Y	Y	OK	OK		
1600-16	1280-32	N	N	Y	Y	OK	OK	61	
1600-16	1600-16	CAP	CAP	N	N	*streaks in window	*streaks in window		
1600-16	1600-16	CAP	N	N	N	light snow in window	OK		
1600-16	1600-16	CAP	N	Y	Y	streaks in window	OK		
1600-16	1600-16	N	CAP	N	N	OK	OK		
1600-16	1600-16	N	CAP	Y	Y	OK	light snow in window		
1600-16	1600-16	N	N	Y	Y	OK	OK	70	
1600-16	1600-24	N	N	N	N	OK	snow		
1600-16	1600-32	N	N	N	N	OK	snow		
1600-16	FP	CAP	N	Y	Y	OK	OK	67	50
1600-16	FP	N	N	Y	Y	OK	OK		
1600-24	FP	N	N	N	N	OK	OK		
1600-24	FP	N	N	Y	Y	light snow	light snow		
1600-32	1600-32	N	N	N	N	snow	light snow		
1600-32	640-32	N	N	N	N	snow	OK		
1600-32	FP	CAP	N	N	N	streaks	streaks		
1600-32	FP	N	N	N	N	OK	OK		
1600-32	FP	N	N	Y	N	light snow	light snow		
1600-32	FP	Y	N	N	N	light streaks	light streaks		
VP	1600-16	N	N	Y	Y	OK	OK		
VP	1600-32	N	N	N	N	snow	snow		

2.5.2 Maximum Display/Capture Performance

It is not practical to test all cases, or even a broad sub-set of cases. So here are a sample of corner cases. The test show that it would be no problem to support a single channel 1600 x 1200 16 bpp DVI display at 70 Hz with no video capture, but if you wanted to capture a 1024 x 768 60 Hz RGB you should drop down to 8 bpp or 1280 x 1024. Or, for another example, dual 1280 x 1024 24 bpp displays might be touchy, but dual 1024 x 768 24 bpp displays would be easy, even if capturing video to one channel.

The format here is the DVI channel mode, the VGA channel mode, and any video windows.

The method used was to setup a scenario, and then see how high we could bump the refresh rate before artifacts appeared. If the display appeared clean in a 10-15 second gaze, then they passed. We used moving video for capture, and kept a PCI access loop running on display memory. We did NOT have the drawing engine running during these tests. It may be that the display could be acceptable at higher rates, because we rejected any noticeable artifacts, even tiny amounts of snow. But, as mentioned before, differences in usage (like activating the drawing engine) could reveal hitherto unnoticed aberrations.

Test notes:

In single channel mode the DVI and the VGA outputs are identical.

1600 x 1200 GTF timing is only supported on the VGA output in single channel mode.

1280 x 1024 video capture is possible but iffy. Moving data is likely to breakup. PCI access may cause snow or streaks.

There is only one capture channel. Sending the capture channel to both display channels simultaneously degrades performance considerably.

Lower pixel depth (8 bpp instead of 32 bpp) enhance performance considerably. There is only a small performance difference between 24 and 32 bpp.

Test Summary:

Supported modes include (see table next page):

Single 1600 x 1200, 8 or 16 bpp, 70 Hz, DVI or VGA

Single 1280 x 1024, 24 or 32 bpp, 70 Hz, DVI or VGA

Dual 1280 x 1024, 8 or 16 bpp, 70 Hz, DVI and VGA

Dual 1024 x 768, 24 or 32 bpp, 70 Hz, DVI and VGA

Video capture of up to 1024 x 768 into any 8 bpp single channel display

Notes:

DVI or VGA mode: xx-yy-zz, where
xx = format is: 1600 = 1600x1200, 1280 = 1280x1024, 1024 = 1024x768, 800 = 800x600 and 640 = 640x480
yy = bpp, 8, 16, 24, or 32
zz = vertical refresh freq

DVI or VGA Window: xx-zz, bpp always = 16
VGA=DVI for single channel mode

Max display rates test monitors accepted:
DVI: 1600 @ 62 Hz or 1280 @ 85 Hz
VGA: 1600 @ 77 Hz or 1280 @ 86 Hz

All timings are GTF

DVI / VGA refresh rates shown are the maximum possible for the configuration before artifacts appeared. All Window tests used moving video. All tests were with active access to memory bus but drawing engine was not active.

Table 2-6 Maximum Display/Capture Format Capabilities

DVI mode	VGA mode	DVI Window	VGA Window
1600-8-63	VGA=DVI	1024-75	VGA=DVI
1600-8-73	VGA=DVI	640-60	VGA=DVI
1600-8-77+	VGA=DVI	NONE	VGA=DVI
1600-16-48	VGA=DVI	1024-75	VGA=DVI
1600-16-62	VGA=DVI	640-60	VGA=DVI
1600-16-77+	VGA=DVI	NONE	VGA=DVI
1280-8-85+	VGA=DVI	1024-75	VGA=DVI
1280-8-85+	VGA=DVI	640-60	VGA=DVI
1280-8-85+	VGA=DVI	NONE	VGA=DVI
1280-32-52	VGA=DVI	1024-75	VGA=DVI
1280-32-63	VGA=DVI	640-60	VGA=DVI
1280-32-75	VGA=DVI	NONE	VGA=DVI
1600-16-58	1280-32-60	NONE	NONE
1280-8-73	1280-8-74	1024-75	NONE
1280-8-73	1280-8-74	NONE	1024-75
1280-8-45	1280-8-46	1024-75	1024-75
1280-8-85+	1280-8-85+	NONE	NONE
1280-32-59	1280-32-60	NONE	NONE
1024-32-62	1024-32-63	640-75	640-75
1024-32-85+	1024-32-86+	NONE	NONE

2.6 Configuration Information

The basic **Topaz/Tropos/Duros** graphics board includes:

- Silicon Motion SM731 Graphics Processor with 16 MB SDRAM
- 8, 15, 16, 24, or 32 bit/pixel color
- analog video output, dual LVDS (Pn4 only)
- VGA BIOS
- VGA front panel connector

Options include:

- DVI output. VGA connector changes to a DVI-I connector with both VGA and DVI signals sets. A breakout cable is required to obtain both signal sets simultaneously.
- Tropos and Topaz: on-board 3.3V regulator for backplanes which do not have 3.3V

The **Topaz/Stratus/Garnet** graphics board includes the ***Topaz/Tropos/Duros with DVI*** features (above), plus:

- Conexant Bt835 4 input NTSC/PAL/SECAM video digitizer
- Analog Devices AD9882 high speed RGB/YUV/DVI digitizer
- Analog Devices ADV7120 or ADV7123 DAC (secondary VGA)
- THine THC63DV164 DVI encoder
- Configuration EEPROM
- LM75 thermal sensor

Options include:

- Rear Panel I/O – all signals connect to PMC Pn4. Includes custom configurations (see next pages)
- Topaz and Stratus: on-board 3.3V regulator for backplanes which do not have 3.3V

Table 2-7 Standard Front Panel Board Configurations and Connector Utilization

Board Version	Use Breakout Cable(s)	MDSM or MDR20/26 Pinout	DVI Pinout	VGA out Ch 1	VGA out Ch 2	DVI Out Ch 1	LVDS Out Ch 1	LVDS Out Ch 2	NTSC/ PAL Video I/O	RGBHV In	DVI In
TopazPMC/1V				VGA 1	VGA 2		PMC Pn4	PMC Pn4			
TopazPMC/1L	VGA: A31-00735-2012 MDR: A31-00735-4012	26C		VGA 1			MDR26	MDR26	VGA 1 comp out		
TopazPMC/1D	DVI: A31-00735-1012 MDR: A31-00735-3012	20A	D1	DVI-I	DVI-I	DVI-I	PMC Pn4	PMC Pn4	MDR20 video out only		
TopazPMC/2A	DVI: A31-00735-1012 MDR: A31-00735-3012	20A	D1	DVI-I	DVI-I	DVI-I	PMC Pn4	PMC Pn4	MDR20	MDR20	
TopazPMC/2B	DVI: A31-00735-1012 MDR: A31-00735-3012	20A	D2	DVI-I	DVI-I		PMC Pn4	PMC Pn4	MDR20 video out only		DVI-I
TopazPMC/2C	DVI: A31-00735-1012 MDR: A31-00735-5012	20B	D1	DVI-I	DVI-I	DVI-I	PMC Pn4	PMC Pn4			MDR20
TopazPMC/2L	VGA: A31-00735-2012 MDR: A31-00735-8012	26A		VGA 1		PMC Pn4	MDR26		MDR26	MDR26	
TopazPMC/2N	VGA: A31-00735-2012 MDR: A31-00735-7012	26B		VGA 1		PMC Pn4	MDR26				MDR26
TopazPMC/2M	DVI: A31-00735-1012 MDR: A31-00735-3012	20A	D1	DVI-I	DVI-I	DVI-I	PMC Pn4	PMC Pn4	MDR20	MDR20	PMC Pn4
TroposPMC/1V				VGA 1			PMC Pn4	PMC Pn4			
TroposPMC/1D	DVI: A31-00735-1012					DVI-I	PMC Pn4	PMC Pn4			
StratusPMC/1D	DVI: A31-00735-1012 MDSM: A31-00735-0036		D1	DVI-I	DVI-I	DVI-I	PMC Pn4	PMC Pn4	MDSM video out only		
StratusPMC/2A	DVI: A31-00735-1012 MDSM: A31-00735-0036	MDSMA	D1	DVI-I	DVI-I	DVI-I	PMC Pn4	PMC Pn4	MDSM	MDSM	
StratusPMC/2B	DVI: A31-00735-1012 MDSM: A31-00735-0036	MDSMA	D2	DVI-I	DVI-I		PMC Pn4	PMC Pn4	MDSM video out only		DVI
StratusPMC/2C	DVI: A31-00735-1012 MDSM: A31-00735-6012	MDSMB	D1	DVI-I	DVI-I	DVI-I	PMC Pn4	PMC Pn4			MDSM
StratusPMC/2M	DVI: A31-00735-1012 MDSM: A31-00735-0036	MDSMA	D1	DVI-I	DVI-I	DVI-I	PMC Pn4	PMC Pn4	MDSM	MDSM	PMC Pn4

Table 2-8 Standard Rear Panel Board Configurations and I/O Assignments

	Pinout table	Dual LVDS Out Ch 1 & 2	VGA Out Ch 1	VGA Out Ch 2	DVI Out Ch 1	DVI In	Composite/ S-Video/ NTSC/PAL or Analog RGB In	Composite/ S-Video/ NTSC/PAL Out	Compatibility
TopazPMC/1R2 (DVI Out)	3.20.4	Pn4 Pin Group 1	Pn4 Pin Group 3		Pn4 Pin Group 2				TroposPMC/RIO2 DurosPMC
TopazPMC/1R/RT (RG-101 Compatible VGA)	3.20.10		Pn4 Pin Group 6						
TopazPMC/2R3 (DVI Out / Analog RGB In)	3.20.5	Pn4 Pin Group 1	Pn4 Pin Group 3		Pn4 Pin Group 2		Pn4 Pin Group 4	Pn4 Pin Group 5	StratusPMC/RIO3 GarnetPMC/RIO6
TopazPMC/2R4 (DVI In or Analog RGB In)	3.20.5	Pn4 Pin Group 1	Pn4 Pin Group 3			Pn4 Pin Group 2	Pn4 Pin Group 4	Pn4 Pin Group 5	StratusPMC/RIO4 GarnetPMC/RIO7
TopazPMC/2R8 (Second VGA Out / Analog RGB In)	3.20.6	Pn4 Pin Group 1	Pn4 Pin Group 3	Pn4 Pin Group 2			Pn4 Pin Group 4	Pn4 Pin Group 5	StratusPMC/RIO5 GarnetPMC/RIO8
TopazPMC/2R9 (Second VGA Out / DVI In)	3.20.8	Pn4 Pin Group 1	Pn4 Pin Group 3	Pn4 Pin Group 2		Pn4 Pin Groups 4 and 5			GarnetPMC/RIO9
TopazPMC/2R10 (DVI Out / DVI In)	3.20.7	Pn4 Pin Group 1	Pn4 Pin Group 3		Pn4 Pin Group 2	Pn4 Pin Groups 4 and 5			GarnetPMC/RIO10
TopazPMC/2R12 LVDS Out / VGA Out)	3.20.9	Pn4 Pin Group 1	Pn4 Pin Group 3						

See Section 3.20 for more information about connection to Pn4

Table 2-9 Front Panel Board Model Compatibility

TopazPMC/1V TopazPMC/1D TopazPMC/1D TopazPMC/2A-C, L, N	3.20.3	Pn4 Pin Group 1							TroposPMC/1V TroposPMC/1D StratusPMC/1D
TopazPMC/2 L, N	N/A								
TopazPMC/2M	3.20.4	Pn4 Pin Group 1				Pn4 Pin Group 2			

2.6 Software Support

Rastergraf provides a broad range of software support. The following table shows the current availability. Please contact Rastergraf Sales for special requirements.

Table 2-10 Software

Software	Operating System			
	Linux	**VxWorks**	**Windows 2000, XP**	**LynxOS 4**
X Window System	XFree86 4.3	XFree86 4.3		XFree86 4.3
Video Input Extension	bttv	bttv	btwincap	bttv
BIOS (supports analog RGBHV, sync-on-green, and DVI)	VGA (x86)		VGA	n/a
SDL (Graphics Subroutine Library)	yes	yes		yes
WindML (runs under SDL)		yes		yes
BIST (runs under SDL)		yes		yes

Chapter 3
Connector Pinouts and Cable Information

3.1 Introduction

A variety of front panel connectors and both standard and breakout cables are required for the Topaz, Stratus, and Tropos boards and are covered in the following sections. See Table 3-1 (two pages on) for a guide to the chapter's contents. Also, see Section 2.5 for board part numbers and related information.

The Topaz/Stratus/Tropos DVI-I breakout cable splits out DVI, primary VGA, and with the unused DVI dual link pins, secondary VGA. The Topaz/Stratus MDSM or MDR20 Video I/O breakout cable splits out video in and out into BNC and/or S-Video connections.

The Garnet and Duros use only PMC Pn4 rear panel connectors. At this time, there are no cables, breakouts, or PIMs for use with PMC Pn4.

The Topaz, Stratus, and Tropos can also be ordered in rear panel configurations.

Rastergraf can supply you with the breakout and extension cables that are described in this chapter. Please contact Rastergraf sales for any assistance you may need.

Cable Sources

Rastergraf uses an outside contractor to build its production cables:

Lynn Products, Inc. http://www.lynnprod.com

Table 3-1 Front Panel Signal Definitions

Pn4/Schematic Name	Function
LVDSA_TX3P, LVDSB_TX3P, etc.	LVDS Ch A and Ch B (respectively) signals. LVDSA_TX3P/ LVDSA _TX3N would make up a high-speed differential pair.
DVID_TXCP, etc. DVIB_TXCP, etc.	DVI In signals. DVID_TXCP/DVID_TXCN would make up a high-speed differential pair. DVI Out signals. DVIB_TXCP/DVIB_TXCN would make up a high-speed differential pair. Note that all lines must be the same length and each pair must use twisted pair with shield cabling. Each shield must be separately tied to ground, not all shields together and then to ground.
VIN3/HS_HSYNC, etc.	This is a signal pin shared between the Bt835 NTSC/PAL/SECAM decoder and the high-speed AD9882 RGBHV decoder. VIN indicates a Bt835 video input multiplexer input. Numeral indicates which physical port. VIN3 would be the fourth (0-3) input. HS_ means high-speed signal. HSYNC is, of course, horizontal sync input.
GREEN, etc. or Primary Green, etc. SO_GREEN, etc. or Secondary Green, etc.	Part of the Primary VGA output. Part of the Secondary VGA output. RED, GREEN, and BLUE must use 75-ohm coax. Each shield must be separately tied to ground, not all shields together and then to ground. HSYNC and VSYNC should each be twisted pair with a ground. SDC and SDA can be straight or twisted pairs.
COUT, etc.	Part of the component or composite video output signal set.

Table 3-2 Front and Rear Panel Connector Usage

Section	Connector Type	Cable P/N	Pinout(s)	Board Version(s)	Where Used
3.2	VGA			TopazPMC/1V TroposPMC/1V	Board side connector
3.3	DVI-I		D1, D2	TopazPMC/1D TopazPMC/2x StratusPMC/1D StratusPMC/2x TroposPMC/1D	Board side connector
3.4	MDR20		MDR20A, B	TopazPMC/2A-C, M	Board side connector
3.5	MDR26		MDR26A-C	TopazPMC/1L, 2L, 2N	Board side connector
3.6	MSDM-15		MDSMA, B	StratusPMC/2x	Board side connector
3.7	S-Video			TopazPMC/2A, B, M StratusPMC/2A, 2M	Breakout Cables
3.8	VGA	A31-00599-1012		TroposPMC/1V	VGA to VGA Cable
3.9	S-Video, BNC	A31-00709-1003, VAD44		TopazPMC/2A, B, M StratusPMC/2A, 2M	S-Video Adapters
3.10	DVI-I, VGA	A31-00735-1012	D2	Topaz/ Stratus/Tropos	Multifunction Breakout Cable
3.11	DVI, VGA	88741-8700, A31-00599-5012	D1	TopazPMC/1D StratusPMC/1D StratusPMC/2x TroposPMC/1D	DVI to VGA Adapters
3.12	VGA	A31-00735-2012	Topaz VGA	Topaz PMC/1L, 2L, 2N	VGA Breakout Cable
3.13	MDR20	A31-00735-3012	MDR20A	TopazPMC/2A, B, M	Video I/O Breakout Cable
3.14	MDR20	A31-00735-5012	MDR20B	TopazPMC/2C	DVI In Breakout Cable
3.15	MDR26	A31-00735-8012	MDR26A	Topaz PMC/2L	Video I/O + LVDS Out Breakout Cable
3.16	MDR26	A31-00735-7012	MDR26B	Topaz PMC/2N	DVI In + LVDS Out Breakout Cable
3.17	MDR26	A31-00735-4012	MDR26C	Topaz PMC/1L	LVDS Extension Cable
3.18	MSDM-15	A31-00735-0036	MDSMA	StratusPMC/2A, 2M	Video I/O Breakout Cable
3.19	MSDM-15	A31-00735-6012	MDSMB	StratusPMC/2C	DVI In Breakout Cable
3.20	2 row x 64 PMC		Pn1, Pn2, Pn4	All	PMC bus to host rear panel I/O

3.2 VGA Connector

Analog graphics output is provided on a standard VGA style compressed 15 pin D-Sub and is used with an "Autoscan" type monitor. You must use the correct initialization, since a VGA monitor depends on the sync polarities to determine operating frequency. The polarities of the Vertical/Composite Sync and Horizontal Sync are controlled by the SM731 graphics controller chip (see Section 5.2). ***See the* Note *in Section 4.7 concerning composite sync on green and RGBHV video out modes.*** If you have problems, please contact Rastergraf for assistance.

The R, G, and B video outputs are driven by the SM731 graphics controller chip which is capable of driving terminated cable (75 ohms) to standard RS-330/IRE levels. Cable length should be limited to 50 feet unless you use low loss RG-59.

If you really want to roll you own, the PMC board side VGA connector is an AMP 788574-1. Be sure to use 75-ohm coax for the R, G, B. You can use TP or coax on H, and V. A cable that would work is Mogami W3206-8 (http://www.mars-cam.com/ccd/mogami/digital3.html).

Important Note

Because two VGA connectors are a tight fit on the TopazPMC/1V, some VGA connector moldings are too wide to allow two cables to be plugged in simultaneously. Rastergraf can supply cables that are known to fit. The cable part number is A31-00599-1012. See Section 3.8.

Table 3-3 Analog (VGA) Video Connector Pinout

VGA Pin	Description	Ground Type	Cable Type
1	Red		75 ohm Coax with pin 6 Ground
2	Green		75 ohm Coax with pin 7 Ground
3	Blue		75 ohm Coax with pin 8 Ground
4	VOUT *		75 ohm Coax with pin 5 Ground
5	DDC Ground	Circuit Ground	
6	Red Ground	Circuit Ground	
7	Green Ground	Circuit Ground	
8	Blue Ground	Circuit Ground	
9	Fused +5 Volts, .25A max		
10	Sync Ground	Circuit Ground	
11	Ground	Circuit Ground	
12	DDCDA		Twisted Pair with pin 10 Ground
13	HSYNC		Twisted Pair with pin 5 Ground
14	VSYNC		Twisted Pair with pin 10 Ground
15	DDCCK		Twisted Pair with pin 5 Ground
-	Connector Shell	Chassis Ground	
-	Outer Shield (Cable Jacket)	Chassis Ground	

*Note that Pin 4 is only used only on TopazPMC

Warning:

The Chassis Ground **MUST NOT BE CONNECTED** to Circuit Ground.

3.3 DVI-I Connector

Topaz, Stratus, and Tropos boards that support DVI use the industry standard DVI-I (analog/digital) connector which carries both the DVI digital and the traditional RGBHV analog graphics signals. See http://www.ddwg.org/ for more information. The TopazPMC/2 and StratusPMC bring out the second VGA channel on some DVI spare pins (see next page).

The DVI protocol uses the TMDS encoded data format. Each of the three differential data pairs encodes nine digital video (TTL) signals. A separate pair carries the clock. DVI requires all pairs be closely matched in length..

Note that there is only one DVI channel, It is driven by an external DVI encoder connected the SM731 24-bit FP channel output. The encoder is a THine THC63DV164 DVI transmitter (http://www.thine.co.jp). To ensure best quality, we strongly urge you to obtain commercially manufactured cables and/or adapters that are available from Rastergraf, Molex, and other well-known suppliers.

Table 3-4 Tropos DVI-I Connector (Pinout D1)

DVI-I Pin	Description
1	DVI_TX2L
2	DVI_TX2H
3	DVI_TX2 Shield/Ground
6	DDCCK
7	DDCDA
8	Vertical Sync
9	DVI_TX1L
10	DVI_TX1H
11	DVI_TX1 Shield/Ground
14	Fused +5 Volts, .25A max
15	Ground
17	DVI_TX0L
18	DVI_TX0H
19	DVI_TX0 Shield/Ground
22	DVI_TXC Shield/Ground
23	DVI_TXCH
24	DVI_TXCL
4, 5, 12, 13, 16, 20, 21	n/c
C1	Red
C2	Green
C3	Blue
C4	Horizontal Sync
C5	Analog Ground

TopazPMC/2 and StratusPMC Modified DVI-I Connector

The TopazPMC/2 and StratusPMC use the standard DVI-I connector on the front panel. However, in order to get access to the second VGA port, they use the DVI pins reserved for super-high-resolution dual-link DVI. Dual link will never be supported on TopazPMC/2 and StratusPMC.

Note that there is only one DVI channel, It is driven by an external DVI encoder connected the SM731 24-bit FP channel output.

A breakout cable (A31-00749-1012) is available. See Section 3.10 for more information.

The table below shows the usage of the DVI-I pins for the TopazPMC/2 and StratusPMC. Non-standard usages are shown in ***bold italic***.

Table 3-5 TopazPMC/2 and StratusPMC DVI-I Connector (Pinout D2)

DVI-I Pin	Description
1	DVI_TX2L
2	DVI_TX2H
3	DVI_TX2 Shield/Ground
4	***Secondary VGA Red***
5	***Secondary VGA Vertical Sync***
6	DVI/ Primary VGA DDCCK
7	DVI/ Primary VGA DDCDA
8	Primary VGA Vertical Sync
9	DVI_TX1L
10	DVI_TX1H
11	DVI_TX1 Shield/Ground
12	***Secondary VGA Green***
13	***Secondary VGA DDCCK***
14	Fused +5 Volts, .25A max
15	Ground
16	***Secondary VGA DDCDA***
17	DVI_TX0L
18	DVI_TX0H
19	DVI_TX0 Shield/Ground
20	***Secondary VGA Blue***
21	***Secondary VGA Horizontal Sync***
22	DVI_TXC Shield/Ground
23	DVI_TXCH
24	DVI_TXCL
C1	Primary VGA Red
C2	Primary VGA Green
C3	Primary VGA Blue
C4	Primary VGA Horizontal Sync
C5	Analog Ground

3.4 MDR20 Connector

The TopazPMC/2 uses a 20-pin 3M# 10220-1210VE female MDR connector for Video I/O (VI/O). Rastergraf can supply a breakout cable that provides a set of BNCs and S-Video connectors. No BNC to S-Video adapters are required.

Table 3-6 Video I/O (VI/O) Front Panel Connector (Pinouts 20A & 20B)

MDR Pin Number	MDR20 Pinout 20A	MDR20 Pinout 20B
1, 11	Ground	Ground
2	YOUT	DVI_IN_ TXCLKN
12	VOUT	DVI_IN_ TXCLKP
3	YIN_VIN0/HS_RED	DVI_IN_ TX1P
13	VIN1/HS_GREEN	DVI_IN_ TX1N
4, 14	Ground	Ground
5	COUT	DVI_IN_TX2N
15	CIN/HS_VSYNC	DVI_IN_TX2P
6	VIN2/HS_BLUE	DVI_IN_ TX0P
16	VIN3HS_HSYNC	DVI_IN_ TX0N
7	Ground	Ground
17	F5V	F5V
8-10, 18-20	n/c	n/c

3.4.1 MDR20 Pinout 20A – NTSC/PAL or RGBHV In, NTSC/PAL Out

The ***MDR20 Pinout 20A*** supports dual use pins. The NTSC/PAL and high-speed RGB input signals are connected together on the board. They are shown in the table to illustrate the different capabilities of the board.

NTSC/PAL Input

VIN0-VIN3 are composite NTSC/PAL Inputs and CIN is an input dedicated to Chrominance. VIN 0 can be used with the CIN for S-Video input applications. Each input is connected to the digitizing chips by a .1 uF input capacitor and presents a (DC) 75-ohm impedance to the driving source. No low pass filtering is done on the signals. The Bt835 multiplexer is ***not*** break-before-make, so inputs will be *momentarily* connected together when switching from one input to another. YOUT (luminance or brightness), VOUT, and COUT (chrominance or color) are the outputs of the SM731 VGA to NTSC/PAL encoder.

Loopback Mode

Note that as a test feature, a control bit can make the VOUT loopback to VIN1. The only time the loopback should be enabled is when VIN1 is not otherwise connected.

RGBHV Input

The MDR20 connector can be used to connect to the high-speed (HS) digitizer, which acquires RGBHV or RGB + SOG, up to 1280 x 1024 at 120 MHz. The table above shows the ***MDR20 Pinout 20A*** pin definitions share pins between the NTSC/PAL digitizer and the high-speed digitizer. The connections are wired in parallel except for that the 75-ohm terminations on VIN3 and CIN are removed in HS mode.

3.4.2 MDR20 Pinout 20B – DVI Input

The MDR20 connector can also be used to connect to the DVI inputs of the high-speed AD9882 digitizer at up to 1024 x 768. The table above shows the ***MDR20 Pinout 20B*** pin definitions. Using this mode is definitely a second choice to using the DVI-I connector's (usually) DVI output function for digitizing. However, if you still need DVI out, then MDR20 is the best way to provide DVI In.

3.5 MDR26 Connector

The TopazPMC/1L uses a 26-pin 3M #10226-1210VE female MDR26 connector to provide single high resolution (1600x1200) or dual medium resolution (1024x768) LVDS output(s) on the PMC front panel. The TopazPMC/2L and /2N can provide a single medium resolution (1024x768) LVDS output plus a variety of NTSC/PAL, high-speed RGB, or DVI input functions.

Table 3-7 Video I/O (VI/O) Front Panel Connector (Pinouts 26A-26C)

MDR26 Pin Number	MDR26 Pinout 26A	MDR26 Pinout 26B	MDR26 Pinout 26C
1, 14	Ground	Ground	Ground
2	YOUT	DVI_IN_ TXCLKN	FLVDSB_TX3P
15	VOUT	DVI_IN_ TXCLKP	FLVDSB_TX3N
3	YIN_VIN0/HS_RED	DVI_IN_ TX1P	FLVDSB_TXCP
16	VIN1/HS_GREEN	DVI_IN_ TX1N	FLVDSB_TXCN
4	Ground	Ground	FLVDSB_TX2P
17	Ground	Ground	FLVDSB_TX2N
5	COUT	DVI_IN_TX2N	FLVDSB_TX1P
18	CIN /HS_VSYNC	DVI_IN_TX2P	FLVDSB_TX1N
6	VIN2/HS_BLUE	DVI_IN_ TX0P	FLVDSB_TX0P
19	VIN3/HS_HSYNC	DVI_IN_ TX0N	FLVDSB_TX0N
7	Ground	Ground	Ground
20	F5V	F5V	F5V
8	FLVDSA_TX3P	FLVDSA_TX3P	FLVDSA_TX3P
21	FLVDSA_TX3N	FLVDSA_TX3N	FLVDSA_TX3N
9	FLVDSA_TXCP	FLVDSA_TXCP	FLVDSA_TXCP
22	FLVDSA_TXCN	FLVDSA_TXCN	FLVDSA_TXCN
10	FLVDSA_TX2P	FLVDSA_TX2P	FLVDSA_TX2P
23	FLVDSA_TX2N	FLVDSA_TX2N	FLVDSA_TX2N
11	FLVDSA_TX1P	FLVDSA_TX1P	FLVDSA_TX1P
24	FLVDSA_TX1N	FLVDSA_TX1N	FLVDSA_TX1N
12	FLVDSA_TX0P	FLVDSA_TX0P	FLVDSA_TX0P
25	FLVDSA_TX0N	FLVDSA_TX0N	FLVDSA_TX0N
13, 26	Ground	Ground	Ground

3.5.1 MDR26 Pinout 26A – Video In, Video Out, Ch 1 LVDS Out

The ***MDR26 Pinout 26A*** supports dual use pins. The NTSC/PAL and high-speed RGB video input signals are connected together on the board. They are shown in the table to illustrate the different capabilities of the board.

NTSC/PAL Input

VIN0-VIN3 are composite NTSC/PAL Inputs and CIN is an input dedicated to Chrominance. VIN 0 can be used with the CIN for S-Video

input applications. Each input is connected to the digitizing chips by a .1 uF input capacitor and presents a (DC) 75-ohm impedance to the driving source. No low pass filtering is done on the signals. The Bt835 multiplexer is ***not*** break-before-make, so inputs will be *momentarily* connected together when switching from one input to another. YOUT (luminance or brightness), VOUT, and COUT (chrominance or color) are the outputs of the SM731 VGA to NTSC/PAL encoder.

Loopback Mode

Note that as a test feature, a control bit can make the VOUT loopback to VIN1. The only time the loopback should be enabled is when VIN1 is not otherwise connected.

RGBHV Input

The MDR26 connector can be used to connect to the high-speed (HS) digitizer, which acquires RGBHV or RGB + SOG, up to 1280 x 1024 at 120 MHz. The table above shows the ***MDR26 Pinout 26A*** pin definitions share pins between the NTSC/PAL digitizer and the high-speed digitizer. The connections are wired in parallel except for that the 75-ohm terminations on VIN3 and CIN are removed in HS mode.

3.5.2 MDR26 Pinout 26B – DVI Input, Ch 1 LVDS Out

The table above shows the ***MDR26 Pinout 26B*** pin definitions which enable the DVI inputs of the high-speed AD9882 digitizer at up to 1024 x 768. Using this mode is definitely a second choice to using the DVI-I connector's (usually) DVI output function for digitizing.

3.5.3 MDR26 Pinout 26C – Ch 1 and CH 2 LVDS Out

The table above shows the ***MDR26 Pinout 26C*** pin definitions which enable the both LVDS ports to be connected. This can support dual 1024 x 768 or a single dual-link 1600x1200 display. For convenience of cabling, the pinout follows the CameraLink frame grabber side basic configuration. Not that there is no actual CameraLink support on any board.

3.6 MDSM Connector

The Stratus uses a 15-pin ITT Cannon MDSM (MDSM-15PE-Z10) connector for the Video I/O (VI/O) front panel connector. Rastergraf can supply a breakout cable that provides a set of 8 BNC connectors.

A BNC (YOUT/COUT) to S-Video DIN can be used to drive S-Video compatible devices. (http://www.a2zcables.com/, part number VY6-1).

The Cannon cable connector part number is MDSM-15SC-Z11-VS1. Cannon also has a 3 foot pigtail cable (CA111972-11) which has the MDSM on one end and uses twisted pair wires. Coax is recommended for video, so this cable will not give you the best results.

Table 3-8 Video I/O (VI/O) Front Panel Connector (Pinouts MDSMA & MDSMB)

MDSM15 Pin Number	MDSM MDSMA	MDSM15 MDSMB
1	YOUT	DVI_IN_ TXCLKN
2	VOUT	DVI_IN_ TXCLKP
3	COUT	DVI_IN_TX2N
4	CIN/HS_VSYNC	DVI_IN_TX2P
5	YIN_VIN0/HS_RED	DVI_IN_ TX1P
6	VIN1/HS_GREEN	DVI_IN_ TX1N
7	VIN2/HS_BLUE	DVI_IN_ TX0P
8	VIN3HS_HSYNC	DVI_IN_ TX0N
9	Ground*	Ground*
10-14	Ground	Ground

* Factory option allows this pin to be wired to fused 5V (F5V)

3.6.1 Pinout MDSMA – NTSC/PAL or RGBHV In, NTSC/PAL Out

The ***Pinout MDSMA*** supports dual use pins. The NTSC/PAL and high-speed RGB input signals are connected together on the board. They are shown in the table to illustrate the different capabilities of the board.

NTSC/PAL Input

VIN0-VIN3 are composite NTSC/PAL Inputs and CIN is an input dedicated to Chrominance. VIN 0 can be used with the CIN for S-Video input applications. Each input is connected to the digitizing chips by a .1 uF input capacitor and presents a (DC) 75-ohm impedance to the driving source. No low pass filtering is done on the signals. The Bt835 multiplexer is ***not*** break-before-make, so inputs will be *momentarily* connected together when switching from one input to another. YOUT (luminance or

brightness), VOUT, and COUT (chrominance or color) are the outputs of the SM731 VGA to NTSC/PAL encoder.

Loopback Mode

Note that as a test feature, a control bit can make the VOUT loopback to VIN1. The only time the loopback should be enabled is when VIN1 is not otherwise connected.

RGBHV Input

The MDSM15 connector can be used to connect to the high-speed (HS) digitizer, which acquires RGBHV or RGB + SOG, up to 1280 x 1024 at 120 MHz. The table above shows the ***Pinout MDSMA*** pin definitions share pins between the NTSC/PAL digitizer and the high-speed digitizer. The connections are wired in parallel except for that the 75-ohm terminations on VIN3 and CIN are removed in HS mode.

3.6.2 Pinout MDSMB – DVI Input

The MDSM15 connector can also be used to connect to the DVI inputs of the high-speed AD9882 digitizer at up to 1024 x 768. The table above shows the ***Pinout MDSMB*** pin definitions. Using this mode is definitely a second choice to using the DVI-I connector's (usually) DVI output function for digitizing.

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3.7 S-Video Connector

We use the S-Video connector for high quality video-in because it is the most common type and is also widely used on PCs and personal video equipment. This makes it easy to get cables and connectors.

Figure 3-1 S-Video Connector

	Pin	Description
 Male connector solder side view	1	Ground (Y)
	2	Ground (C)
	3	Y (Luminance = intensity + Sync.) or Composite Video In
	4	C (Chrominance = color)

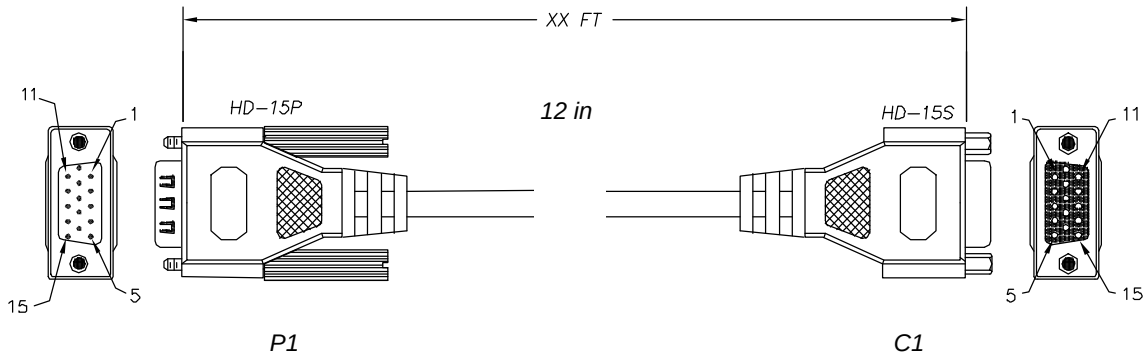
3.8 VGA to VGA Cable

Because two VGA connectors are a tight fit on a PMC board, some VGA connector moldings are too wide to allow two cables to be plugged in simultaneously. Rastergraf can supply cables that are known to fit.

Table 3-9 VGA to VGA Cable (A31-00599-1012)

VGA (P1) Pin	VGA (C2) Pin	Wire Type	Description	
			Function	Name
2	2	75 coax #G	VGA	Green
7	7	75 coax #G	VGA	Green Ground
3	3	75 coax #B	VGA	Blue
8	8	75 coax #B	VGA	Blue Ground
1	1	75 coax #R	VGA	Red
6	6	75 coax #R	VGA	Red Ground
14	14	TP+S #V	VGA	VS
10	10	TP+S #V	VGA	Sync Ground
13	13	TP+S #H	VGA	HS
11	11	TP+S #H	VGA	Ground
12	12	straight	DVI/VGA	SDA
15	15	straight	DVI/VGA	SCL
5	5	straight	DVI/VGA	DDC Ground
9	9	straight	F5V	

Figure 3-2 VGA to VGA Extension Cable (A31-00599-1012)



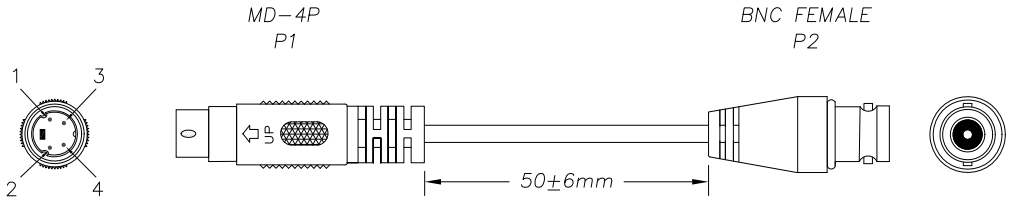
3.9 S-Video Adapter Cables

The TopazPMC/2 VIO breakout cable has two S-Video connectors, one for input and one for output (see Section 3.8). One pin on the input S-Video cable can be used as a standard composite input. The A31-00709-1003 S-Video to BNC adapter cable is supplied for that purpose.

Table 3-10 TopazPMC S-Video to BNC adapter cable (A31-00709-1003)

BNC (P2) Pin	S-Video Pin	Wire Type	Description	
			Function	Name
2	3	75 coax #BLK	Video In	Composite Video In
1	1	75 coax # BLK	Video In	Ground

Figure 3-3 S-Video to BNC Adapter (A31-00709-1003)



The StratusPMC/2 has eight BNCs, of which 2 pairs, VOUT+COUT and YIN_VIN0+CIN, can be used for S-Video. The VAD44 cable (http://store.a2zcable.com/vad44.html) BNC (YOUT/COUT) to S-Video adapter can be used to provide S-Video Input and Output connections.

Table 3-11 StratusPMC BNC to S-Video Adapter Cable (VAD44)

BNC Pin	BNC Connector	S-Video Pin	Wire Type	Description	
				Function	Name
Center	Y	3	75 coax #BLK	Video Out	Y
Shell	Y	1	75 coax # BLK	Video Out	Ground
Center	C	4	75 coax # BLK	Video Out	C
Shell	C	2	75 coax # BLK	Video Out	Ground

Figure 3-4 BNC to S-Video Adapter Cable (VAD44)

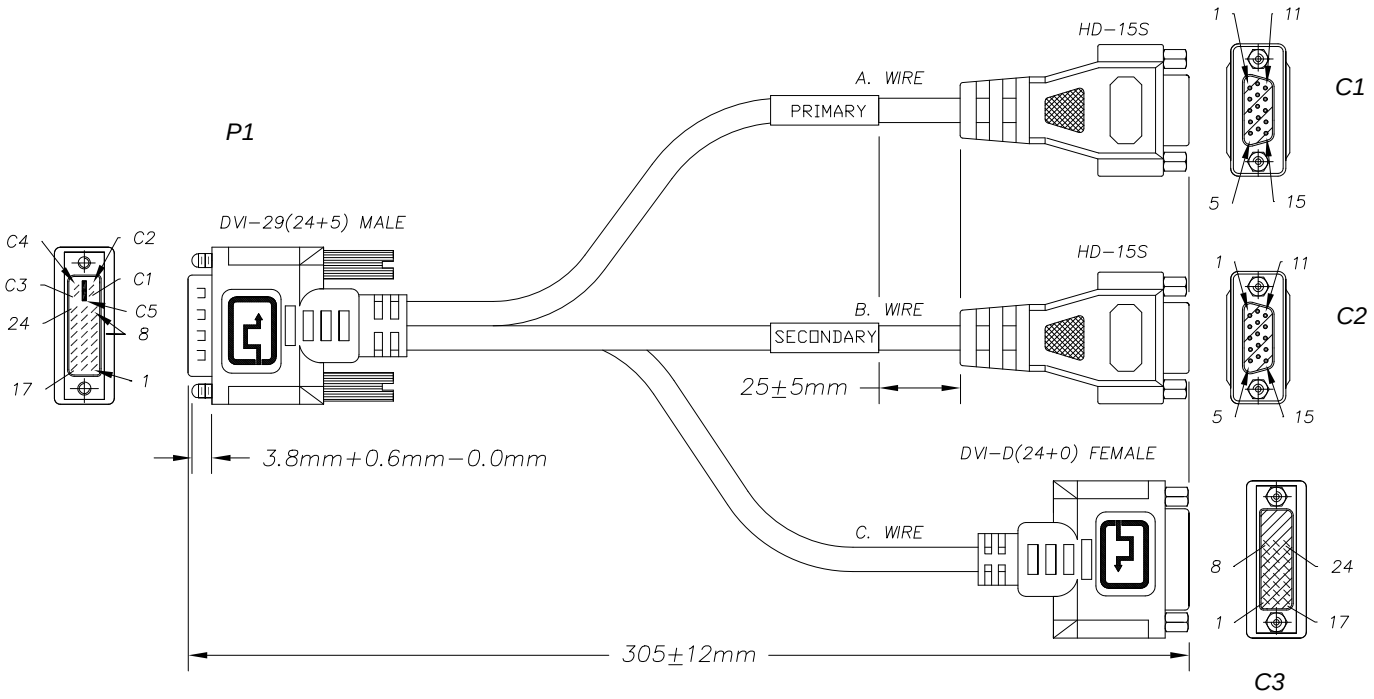
3.10 DVI-I Multifunction Breakout Cable

The DVI-I Multifunction cable addresses the common PMC problem of insufficient front panel space to allow access to all of its functions. Using spare pins on the DVI-I connector, it provides extra signal sets, including DVI and Primary and Secondary VGA.

Note that there is only one DVI channel, It is driven by an external DVI encoder connected the SM731 24-bit FP channel output.

The connectors are shown in the same order as is in the diagram, C1 – C3. Note that P1 is documented in Section 3.3.

Figure 3-5 DVI-I Multifunction Breakout Cable (A31-00735-1012)



3.10.1 C1 – Primary VGA

Table 3-12 C1 - Primary VGA Connector

DVI-I Pin	VGA Pin	Wire Type	Description	
			Function	Name
26 (C2)	2	75 coax #G	VGA	Green
30 (C5)	7	75 coax #G	VGA	Green Ground
27 (C3)	3	75 coax #B	VGA	Blue
29 (C5)	8	75 coax #B	VGA	Blue Ground
25 (C1)	1	75 coax #R	VGA	Red
29 (C5)	6	75 coax #R	VGA	Red Ground
8	14	TP+S #V	VGA	VS
22	10	TP+S #V	VGA	Sync Ground
28 (C4)	13	TP+S #H	VGA	HS
11	11	TP+S #H	VGA	Ground
7	12	straight	DVI/VGA	SDA
6	15	straight	DVI/VGA	SCL
11	5	straight	DVI/VGA	DDC Ground
14	9	straight	F5V	

3.10.2 C2 – Secondary VGA

Table 3-13 C2 - Secondary VGA Connector

DVI-I Pin	VGA Pin	Wire Type	Description	
			Function	Name
12	2	75 coax #G	VGA	Green
15	7	75 coax #G	VGA	Green Ground
20	3	75 coax #B	VGA	Blue
15	8	75 coax #B	VGA	Blue Ground
4	1	75 coax #R	VGA	Red
15	6	75 coax #R	VGA	Red Ground
5	14	TP+S #V	VGA	VS
19	10	TP+S #V	VGA	Sync Ground
21	13	TP+S #H	VGA	HS
3	11	TP+S #H	VGA	Ground
16	12	straight	Sec VGA	SDA
13	15	straight	Sec VGA	SCL
3	5	straight	Sec VGA	DDC Ground
14	9	straight	F5V	

3.10.3 C3 – DVI

Table 3-14 C3 - DVI-D Connector

DVI-I Pin	DVI-D Pin	Wire Type	Description	
			Function	Name
15	15	straight	DVI/VGA	Sync/DDC Ground
7	7	straight	DVI/VGA	SDA
6	6	straight	DVI/VGA	SCL
14	14	straight	F5V	
23	23	TP+S #C	DVI	DVIC_TXCLKP
24	24	TP+S #C	DVI	DVIC_TXCLKN
22	22	TP+S #C	DVI	Pair DCK Ground
18	18	TP+S #0	DVI	DVIC_TX0P
17	17	TP+S #0	DVI	DVIC_TX0N
19	19	TP+S #0	DVI	Pair D0 Ground
10	10	TP+S #1	DVI	DVIC_TX1P
9	9	TP+S #1	DVI	DVIC_TX1N
11	11	TP+S #1	DVI	Pair D1 Ground
2	2	TP+S #2	DVI	DVIC_TX2P
1	1	TP+S #2	DVI	DVIC_TX2N
3	3	TP+S #2	DVI	Pair D2 Ground

3.11 DVI-I to VGA Adapters

On the DVI-optioned boards, a DVI-I connector is used. If you need ONLY the VGA output, a cable-based or modular adapter can be used to supply analog video to a standard VGA ***computer side*** connector. See the diagrams on this and the following page.

Table 3-15 DVI-I to VGA Adapter

DVI-I Pin	VGA Pin	Connector Type	Wire Type	Description	
				Function	Name
2	2	female VGA	75 coax #G	VGA	Green
7	7	female VGA	75 coax #G	VGA	Green Ground
3	3	female VGA	75 coax #B	VGA	Blue
8	8	female VGA	75 coax #B	VGA	Blue Ground
1	1	female VGA	75 coax #R	VGA	Red
6	6	female VGA	75 coax #R	VGA	Red Ground
14	14	female VGA	TP+S #V	VGA	VS
10	10	female VGA	TP+S #V	VGA	Sync Ground
13	13	female VGA	TP+S #H	VGA	HS
11	11	female VGA	TP+S #H	VGA	Ground
12	12	female VGA	straight	DVI/VGA	SDA
15	15	female VGA	straight	DVI/VGA	SCL
5	5	female VGA	straight	DVI/VGA	DDC Ground
9	9	female VGA	straight	F5V	

Figure 3-6 Molex 88741-8700 DVI-I to VGA Adapter

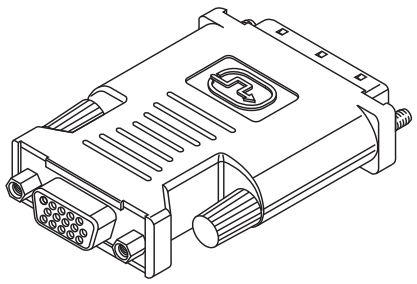
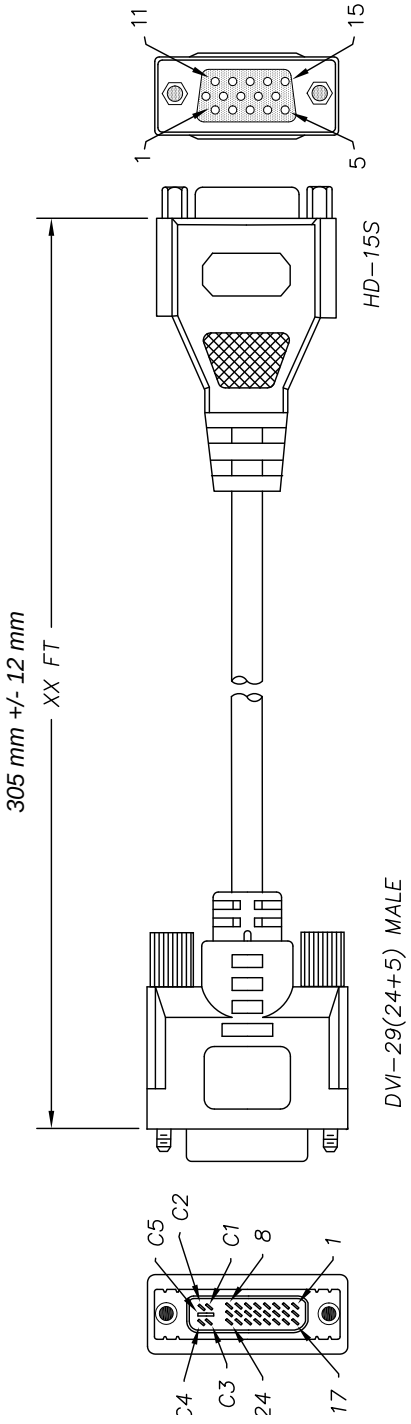


Figure 3-7 DVI to VGA Adapter Cable (A31-00599-5012)



3.12 TopazPMC VGA Breakout Cable

The TopazPMC VGA breakout cable uses a spare pin on the VGA connector to bring out composite video out. It is used on the TopazPMC/1L version, which has VGA out and dual LVDS out. Note that P1 is documented in Section 3.3.

Figure 3-8 TopazPMC VGA Breakput Cable (A31-00735-2012)

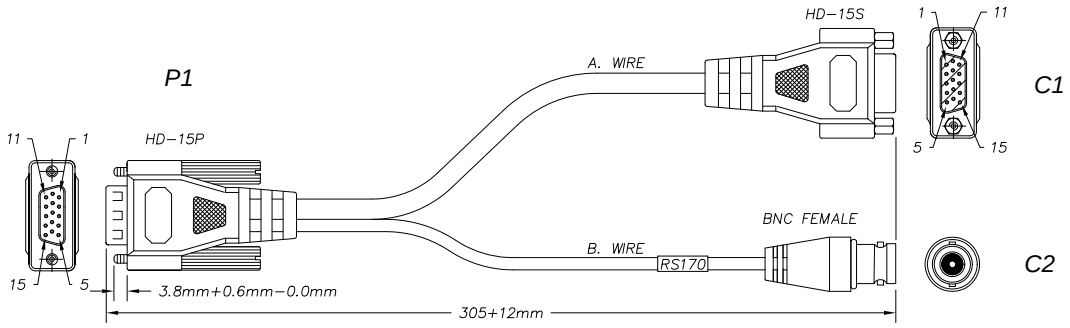


Table 3-16 TopazPMC VGA Breakout Connector

P1 Pin	C1 Pin	C2 Pin	Connector Type	Wire Type	Description	
					Function	Name
2	2		female VGA	75 coax #G	VGA	Green
7	7		female VGA	75 coax #G	VGA	Green Ground
3	3		female VGA	75 coax #B	VGA	Blue
8	8		female VGA	75 coax #B	VGA	Blue Ground
1	1		female VGA	75 coax #R	VGA	Red
6	6		female VGA	75 coax #R	VGA	Red Ground
4		Center	female BNC	75 coax #V	Comp Out	Comp Out
5		Shell	female BNC	75 coax #V	Comp Out	Ground
14	14		female VGA	TP+S #V	VGA	VS
10	10		female VGA	TP+S #V	VGA	Sync Ground
13	13		female VGA	TP+S #H	VGA	HS
11	11		female VGA	TP+S #H	VGA	Ground
12	12		female VGA	straight	DVI/VGA	SDA
15	15		female VGA	straight	DVI/VGA	SCL
5	5		female VGA	straight	DVI/VGA	DDC Ground
9	9		female VGA	straight	F5V	

3.13 TopazPMC Video I/O Breakout Cable

The TopazPMC Video I/O Breakout Cable uses the MDR20 connector to bring in NTSC/PAL/S-Video and high speed RGBHV video inputs and provide composite and S-Video out. It is used on the TopazPMC/2A, B, C, and M versions which have the MDR20 connector documented in Section 3.4. See Section 3.9 for the S-Video to BNC Adapter.

Table 3-17 TopazPMC Video I/O Breakout Cable

MDR20 Pin	Connector Number	Connector Pin	Connector Type	Wire Type	Description	
					Function	Name
13	C6	center	female BNC	75 coax #GRN	Video In	VIN1/HS_GREEN
11	C6	shell	female BNC	75 coax # GRN	Video In	Ground
6	C7	center	female BNC	75 coax #BLU	Video In	VIN2/HS_BLUE
4	C7	shell	female BNC	75 coax # BLU	Video In	Ground
16	C8	center	female BNC	75 coax #VIO	Video In	VIN3/HS_HSYNC
14	C8	shell	female BNC	75 coax # VIO	Video In	Ground
12	C2	center	female BNC	75 coax #BRN	Video Out	VOUT
11	C2	shell	female BNC	75 coax # BRN	Video Out	Ground
3	C54	3	female S-Video In	75 coax #YEL	Video In	YIN_VIN0/HS_RED
1	C54	1	female S-Video In	75 coax # YEL	Video In	Ground
15	C54	4	female S-Video In	75 coax #ORG	Video In	CIN/HS_VSYNC
14	C54	2	female S-Video In	75 coax # ORG	Video In	Ground
2	C13	3	female S-Video Out	75 coax #BLK	Video Out	YOUT
1	C13	1	female S-Video Out	75 coax # BLK	Video Out	Ground
5	C13	4	female S-Video Out	75 coax #RED	Video Out	COUT
4	C13	2	female S-Video Out	75 coax # RED	Video Out	Ground

3.14 TopazPMC DVI In Adapter Cable

The TopazPMC DVI In MDR20 to Female DVI-D Adapter Cable uses the MDR20 connector to bring in high speed DVI In. It is used on the TopazPMC/2A, B, C, and M versions which have the MDR20 connector documented in Section 3.4.

Table 3-18 TopazPMC DVI In Adapter Cable

MDR20 Pin	DVI-D Pin	Wire Type	Description	
			Function	Name
12	23	TP+S #C	DVI	DVID_TXCLKP
2	24	TP+S #C	DVI	DVID_TXCLKN
1	22	TP+S #C	DVI	Pair DCK Ground
6	18	TP+S #0	DVI	DVID_TX0P
16	17	TP+S #0	DVI	DVID_TX0N
7	19	TP+S #0	DVI	Pair D0 Ground
3	10	TP+S #1	DVI	DVID_TX1P
13	9	TP+S #1	DVI	DVID_TX1N
14	11	TP+S #1	DVI	Pair D1 Ground
15	2	TP+S #2	DVI	DVID_TX2P
5	1	TP+S #2	DVI	DVID_TX2N
4	3	TP+S #2	DVI	Pair D2 Ground

3.15 TopazPMC Video I/O + LVDS Breakout Cable

The TopazPMC Video I/O + LVDS Breakout Cable uses the MDR26 connector to bring in NTSC/PAL/S-Video and high speed RGBHV video inputs and provide composite and S-Video out and single-link LVDS out. It is used on the TopazPMC/2L and N versions which have the MDR26 connector documented in Section 3.5. See Section 3.9 for the S-Video to BNC Adapter.

Table 3-19 TopazPMC Video I/O + LVDS Breakout Cable

MDR20 Pin	Connector Number	Connector Pin	Connector Type	Wire Type	Description	
					Function	Name
16	C6	center	female BNC	75 coax #GRN	Video In	VIN1/HS_GREEN
14	C6	shell	female BNC	75 coax # GRN	Video In	Ground
6	C7	center	female BNC	75 coax #BLU	Video In	VIN2/HS_BLUE
4	C7	shell	female BNC	75 coax # BLU	Video In	Ground
19	C8	center	female BNC	75 coax #VIO	Video In	VIN3HS_HSYNC
17	C8	shell	female BNC	75 coax # VIO	Video In	Ground
15	C2	center	female BNC	75 coax #BRN	Video Out	VOUT
14	C2	shell	female BNC	75 coax # BRN	Video Out	Ground
3	C54	3	female S-Video In	75 coax #YEL	Video In	YIN_VIN0/HS_RED
1	C54	1	female S-Video In	75 coax # YEL	Video In	Ground
18	C54	4	female S-Video In	75 coax #ORG	Video In	CIN/HS_VSYNC
17	C54	2	female S-Video In	75 coax # ORG	Video In	Ground
2	C13	3	female S-Video Out	75 coax #BLK	Video Out	YOUT
1	C13	1	female S-Video Out	75 coax # BLK	Video Out	Ground
5	C13	4	female S-Video Out	75 coax #RED	Video Out	COUT
4	C13	2	female S-Video Out	75 coax # RED	Video Out	Ground
8	C9	8	Male MDR26	TP+S #3	LVDS Out	FLVDSA_TX3P
21	C9	21	Male MDR26	TP+S #3	LVDS Out	FLVDSA_TX3N
1	C9	1	Male MDR26	TP+S #3	LVDS Out	Ground
9	C9	9	Male MDR26	TP+S #C	LVDS Out	FLVDSA_TXCP
22	C9	22	Male MDR26	TP+S #C	LVDS Out	FLVDSA_TXCN
14	C9	14	Male MDR26	TP+S #C	LVDS Out	Ground
10	C9	10	Male MDR26	TP+S #2	LVDS Out	FLVDSA_TX2P
23	C9	23	Male MDR26	TP+S #2	LVDS Out	FLVDSA_TX2N
13	C9	13	Male MDR26	TP+S #2	LVDS Out	Ground
11	C9	11	Male MDR26	TP+S #1	LVDS Out	FLVDSA_TX1P
24	C9	24	Male MDR26	TP+S #1	LVDS Out	FLVDSA_TX1N
26	C9	26	Male MDR26	TP+S #1	LVDS Out	Ground
12	C9	12	Male MDR26	TP+S #0	LVDS Out	FLVDSA_TX0P
25	C9	25	Male MDR26	TP+S #0	LVDS Out	FLVDSA_TX0N
13	C9	13	Male MDR26	TP+S #0	LVDS Out	Ground

3.16 TopazPMC DVI In + LVDS Breakout Cable

The TopazPMC DVI In + LVDS Breakout Cable uses the MDR26 connector to bring in DVI and single-link LVDS out. It is used on the TopazPMC/2L and N versions which have the MDR26 connector documented in Section 3.5.

Table 3-20 TopazPMC DVI In + LVDS Breakout Cable

MDR20 Pin	Connector Number	Connector Pin	Connector Type	Wire Type	Description	
					Function	Name
15	C1	23	female DVI-D	TP+S #C	DVI	DVID_TXCLKP
2	C1	24	female DVI-D	TP+S #C	DVI	DVID_TXCLKN
1	C1	22	female DVI-D	TP+S #C	DVI	Pair DCK Ground
6	C1	18	female DVI-D	TP+S #0	DVI	DVID_TX0P
19	C1	17	female DVI-D	TP+S #0	DVI	DVID_TX0N
7	C1	19	female DVI-D	TP+S #0	DVI	Pair D0 Ground
3	C1	10	female DVI-D	TP+S #1	DVI	DVID_TX1P
16	C1	9	female DVI-D	TP+S #1	DVI	DVID_TX1N
14	C1	11	female DVI-D	TP+S #1	DVI	Pair D1 Ground
5	C1	2	female DVI-D	TP+S #2	DVI	DVID_TX2P
18	C1	1	female DVI-D	TP+S #2	DVI	DVID_TX2N
4	C1	3	female DVI-D	TP+S #2	DVI	Pair D2 Ground
8	C2	8	Male MDR26	TP+S #3	LVDS Out	FLVDSA_TX3P
21	C2	21	Male MDR26	TP+S #3	LVDS Out	FLVDSA_TX3N
1	C2	1	Male MDR26	TP+S #3	LVDS Out	Pair L3 Ground
9	C2	9	Male MDR26	TP+S #C	LVDS Out	FLVDSA_TXCP
22	C2	22	Male MDR26	TP+S #C	LVDS Out	FLVDSA_TXCN
14	C2	14	Male MDR26	TP+S #C	LVDS Out	Pair LCK Ground
10	C2	10	Male MDR26	TP+S #2	LVDS Out	FLVDSA_TX2P
23	C2	23	Male MDR26	TP+S #2	LVDS Out	FLVDSA_TX2N
13	C2	13	Male MDR26	TP+S #2	LVDS Out	Pair L2 Ground
11	C2	11	Male MDR26	TP+S #1	LVDS Out	FLVDSA_TX1P
24	C2	24	Male MDR26	TP+S #1	LVDS Out	FLVDSA_TX1N
26	C2	26	Male MDR26	TP+S #1	LVDS Out	Pair L1 Ground
12	C2	12	Male MDR26	TP+S #0	LVDS Out	FLVDSA_TX0P
25	C2	25	Male MDR26	TP+S #0	LVDS Out	FLVDSA_TX0N
13	C2	13	Male MDR26	TP+S #0	LVDS Out	Pair L0 Ground

3.17 TopazPMC LVDS Extension Cable

The TopazPMC LVDS Extension Cable has two male MDR26 connectors. It supports dual-link high resolution or two single-link medium resolution LVDS panels. It is used on the TopazPMC/1L version which has the MDR26 connector documented in Section 3.5.

The cable is the same as the 3M #14B26-SZLB-300-0LC (3 meter with thumbscrews) cable. Note that the connections are not the same at each connector, but rather are cross-wired according to the chart on the next page. By convention, the TopazPMC/1L follows the "Frame Grabber" end, although, of course, it is a display device, not a frame grabber.

Figure 3-9 TopazPMC LVDS Extension Cable (A31-00735-4012)

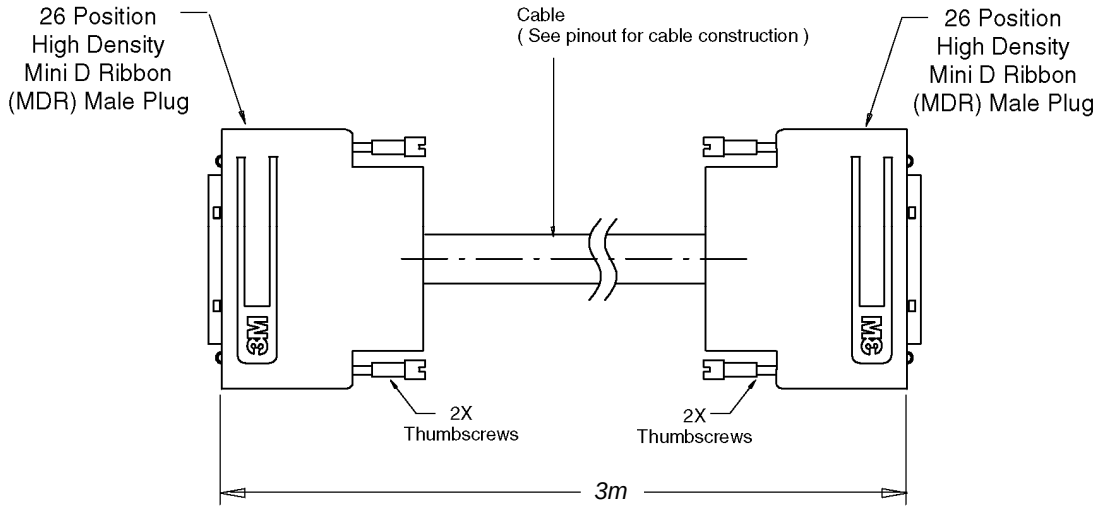


Table 3-21 TopazPMC LVDS Extension Cable (A31-00735-4012)

Topaz side MDR26 Pin	Far end MDR26 Pin	Connector Type	Wire Type	Description	
				Function	Name
2	25	Male MDR26	TP+S #B3	LVDS Out	FLVDSB_TX3P
15	12	Male MDR26	TP+S #B3	LVDS Out	FLVDSB_TX3N
13	14	Male MDR26	TP+S #B3	LVDS Out	Pair BL3 Ground
3	24	Male MDR26	TP+S #BC	LVDS Out	FLVDSB_TXCP
16	11	Male MDR26	TP+S #BC	LVDS Out	FLVDSB_TXCN
26	1	Male MDR26	TP+S #BC	LVDS Out	Pair BLCK Ground
4	23	Male MDR26	TP+S #B2	LVDS Out	FLVDSB_TX2P
17	10	Male MDR26	TP+S #B2	LVDS Out	FLVDSB_TX2N
13	14	Male MDR26	TP+S #B2	LVDS Out	Pair BL2 Ground
5	22	Male MDR26	TP+S #B1	LVDS Out	FLVDSB_TX1P
18	9	Male MDR26	TP+S #B1	LVDS Out	FLVDSB_TX1N
26	1	Male MDR26	TP+S #B1	LVDS Out	Pair BL1 Ground
6	21	Male MDR26	TP+S #B0	LVDS Out	FLVDSB_TX0P
19	8	Male MDR26	TP+S #B0	LVDS Out	FLVDSB_TX0N
13	14	Male MDR26	TP+S #B0	LVDS Out	Pair BL0 Ground
7	20	Male MDR26	TP+S #C0	Term	100 ohm term P
20	7	Male MDR26	TP+S #C0	Term	100 ohm term N
8	19	Male MDR26	TP+S #A3	LVDS Out	FLVDSA_TX3P
21	6	Male MDR26	TP+S #A3	LVDS Out	FLVDSA_TX3N
14	13	Male MDR26	TP+S #A3	LVDS Out	Pair AL3 Ground
9	18	Male MDR26	TP+S #AC	LVDS Out	FLVDSA_TXCP
22	5	Male MDR26	TP+S #AC	LVDS Out	FLVDSA_TXCN
1	26	Male MDR26	TP+S #AC	LVDS Out	Pair ALCK Ground
10	17	Male MDR26	TP+S #A2	LVDS Out	FLVDSA_TX2P
23	4	Male MDR26	TP+S #A2	LVDS Out	FLVDSA_TX2N
14	13	Male MDR26	TP+S #A2	LVDS Out	Pair AL2 Ground
11	16	Male MDR26	TP+S #A1	LVDS Out	FLVDSA_TX1P
24	3	Male MDR26	TP+S #A1	LVDS Out	FLVDSA_TX1N
1	26	Male MDR26	TP+S #A1	LVDS Out	Pair AL1 Ground
12	15	Male MDR26	TP+S #A0	LVDS Out	FLVDSA_TX0P
25	2	Male MDR26	TP+S #A0	LVDS Out	FLVDSA_TX0N
14	13	Male MDR26	TP+S #A0	LVDS Out	Pair AL0 Ground

3.18 StratusPMC Video I/O Breakout Cable

The StratusPMC Video I/O Breakout Cable uses the MDSM15 connector to bring in NTSC/PAL/S-Video and high speed RGBHV video inputs and provide composite and S-Video out. It is used on the StratusPMC versions which have the MDSM connector documented in Section 3.6. See Section 3.9 for the BNC to S-Video Adapter.

Figure 3-10 MDSM to BNC Breakout Cable (A31-00735-0036)

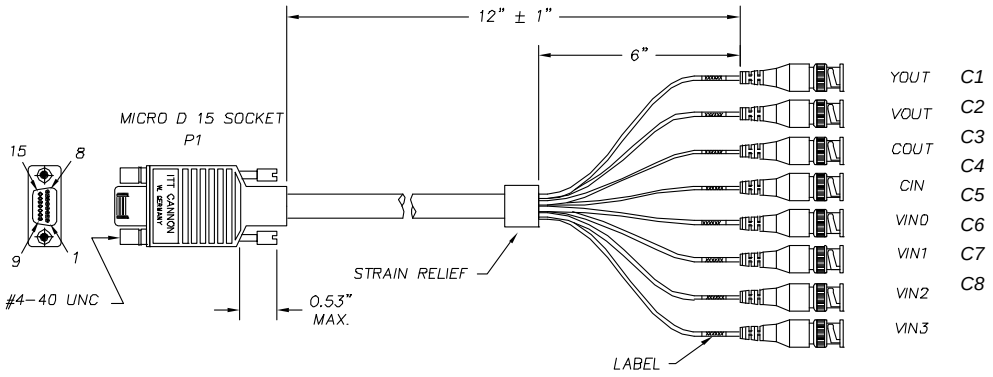


Table 3-22 StratusPMC Video I/O Breakout Cable (A31-00735-0036)

MDSM Pin	Connector Number	Connector Pin	Connector Type	Wire Type	Description	
					Function	Name
1	C1	center	male BNC	75 coax #BLK	Video Out	YOUT
9	C1	shell	male BNC	75 coax # BLK	Video Out	Ground
2	C2	center	male BNC	75 coax #BRN	Video Out	VOUT
9	C2	shell	male BNC	75 coax # BRN	Video Out	Ground
3	C3	center	male BNC	75 coax #RED	Video Out	COUT
10	C3	shell	male BNC	75 coax # RED	Video Out	Ground
4	C4	center	male BNC	75 coax #ORG	Video In	CIN/HS_VSYNC
11	C4	shell	male BNC	75 coax # ORG	Video In	Ground
5	C5	center	male BNC	75 coax #YEL	Video In	YIN_VIN0/HS_RED
12	C5	shell	male BNC	75 coax # YEL	Video In	Ground
6	C6	center	male BNC	75 coax #GRN	Video In	VIN1/HS_GREEN
13	C6	shell	male BNC	75 coax # GRN	Video In	Ground
7	C7	center	male BNC	75 coax #BLU	Video In	VIN2/HS_BLUE
14	C7	shell	male BNC	75 coax # BLU	Video In	Ground
8	C8	center	male BNC	75 coax #VIO	Video In	VIN3HS_HSYNC
15	C8	shell	male BNC	75 coax # VIO	Video In	Ground

3.19 StratusPMC DVI In Adapter Cable

The StratusPMC DVI In MDSM15 to Female DVI-D Adapter Cable uses the MDSM connector to bring in high speed DVI In. It is used on the StratusPMC which have the MDSM connector documented in Section 3.6.

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Table 3-23 StratusPMC DVI In Adapter Cable

MDSM Pin	DVI-D Pin	Connector Type	Wire Type	Description	
				Function	Name
1	24	female DVI-D	75 coax #BLK	Video Out	DVID_TXCLKN
2	23	female DVI-D	75 coax #BRN	Video Out	DVID_TXCLKP
9	22	female DVI-D	75 coax # BRN	Video Out	Ground
3	1	female DVI-D	75 coax #RED	Video Out	DVID_TX2N
4	2	female DVI-D	75 coax #ORG	Video In	DVID_TX2P
11	3	female DVI-D	75 coax # ORG	Video In	Ground
5	10	female DVI-D	75 coax #YEL	Video In	DVID_TX1P
6	9	female DVI-D	75 coax #GRN	Video In	DVID_TX1N
13	11	female DVI-D	75 coax # GRN	Video In	Ground
7	18	female DVI-D	75 coax #BLU	Video In	DVID_TX0P
8	17	female DVI-D	75 coax #VIO	Video In	DVID_TX0N
15	19	female DVI-D	75 coax # VIO	Video In	Ground

3.20 Connections to PMC Pn1, Pn2, and Pn4

All boards are connected to the host CPU via the standard 32-bit PMC Pn1 and Pn2 connectors. Most of the connections go only to the SM731. A few lines go elsewhere on the board for reset, interrupt, and busmode.

See ***Table 2-6*** in Section 2.5 for a hyperlinked listing of boards versus pinouts.

Pn4 Connectors

The Topaz, Stratus, and Tropos versions can be ordered with graphics and video on the PMC Pn4 connector for cases in which no connections to the front panel are allowed. Garnet and Duros use ***only*** the Pn4 connector for I/O. The signal sets presented on the rear panel are the same as the front panel versions. At this time, Rastergraf does not have any Pn4 adapter cards or cables for any board.

All boards except the TopazPMC have dual LVDS digital outputs that are ***only*** available on the Pn4 connector and are always wired to those pins. Thus, even if you order a standard Tropos or Stratus (i.e., without the rear panel I/O option), LVDS will still be on Pn4.

While using Pn4 I/O is very attractive for some applications, there can be some serious difficulties in successfully deploying it. Due to the very high frequency differential signals generated by the DVI and LVDS outputs, great care must be taken in ensuring cleanly routed, equal length traces on the host board between the Pn4 connector and the VME or CPCI backplane connector.

Unless the carrier or host board vendor knew they were routing for the graphics board, this kind of signal routing will not have been done. For best results, Pn4 connections must be inner-layer matched length for DVI and LVDS signals. Other I/Os require inner-layer signal+ground pairs.

Problems with Pn4 I/O are endemic to PMCs, and are not unique either to the boards in this manual in particular or to graphics boards in general. Before committing to Pn4 solution, it is a good idea to contact the carrier or host board vendor so as to obtain the necessary information to make a good decision. Please contact Rastergraf for assistance.

The following table defines the names and uses for the signals on the Pn4 connector.

Table 3-24 Rear Panel Signal Definitions

Pn4/Schematic Name	Function
LVDSA_TX3P, LVDSB_TX3P, etc.	LVDS Ch A and Ch B (respectively) signals. LVDSA_TX3P/ LVDSA _TX3N would make up a high-speed differential pair.
DVID_TXCP, etc. DVIB_TXCP, etc.	DVI In signals. DVID_TXCP/DVID_TXCN would make up a high-speed differential pair. DVI Out signals. DVIB_TXCP/DVIB_TXCN would make up a high-speed differential pair. Note that all lines must be the same length and each pair must use twisted pair with shield cabling. Each shield must be separately tied to ground, not all shields together and then to ground.
REAR_ VIN3/HS_HSYNC, etc.	This is a signal pin shared between the Bt835 NTSC/PAL/SECAM decoder and the high-speed AD9882 RGBHV decoder. VIN indicates a Bt835 video input multiplexer input. Numeral indicates which physical port. VIN3 would be the fourth (0-3) input. HS_ means high-speed signal. HSYNC is, of course, horizontal sync input.
REAR_GREEN, etc. SO_GREEN, etc.	Part of the Primary VGA output. Part of the Secondary VGA output. RED, GREEN, and BLUE must use 75-ohm coax. Each shield must be separately tied to ground, not all shields together and then to ground. HSYNC and VSYNC should each be twisted pair with a ground. SDC and SDA can be straight or twisted pairs.
REAR_COUT, etc.	Part of the component or composite video output signal set.

3.20.1 Pn1 Connector (all boards)

Pin	Signal Name	Signal Name	Pin
1	JTAGTCK	-12V	2
3	Ground	PINTAL	4
5	PINTBL	n/c	6
7	BUSMODE1L	VCC (5V)	8
9	n/c	n/c	10
11	Ground	n/c	12
13	PCICLK	Ground	14
15	Ground	PMCGNTL	16
17	PMCREQL	VCC (5V)	18
19	byp (Vio)	AD31H	20
21	AD28H	AD27H	22
23	AD25H	Ground	24
25	Ground	C/BE3L	26
27	AD22H	AD21H	28
29	AD19H	VCC (5V)	30
31	byp (Vio)	AD17H	32
33	FRAMEL	Ground	34
35	Ground	IRDYL	36
37	DEVSELL	VCC (5V)	38
39	Ground	n/c	40
41	n/c	n/c	42
43	PAR	Ground	44
45	byp (Vio)	AD15H	46
47	AD12H	AD11H	48
49	AD09H	VCC (5V)	50
51	Ground	C/BE0L	52
53	AD06H	AD05	54
55	AD04H	Ground	56
57	byp (Vio)	AD03H	58
59	AD02H	AD01H	60
61	AD00H	VCC (5V)	62
63	Ground	n/c	64

Notes: byp means the pin is connected to a bypass capacitor on the graphics board but is otherwise not used. n/c means no connect – user should not connect to the pin.

3.20.2 Pn2 Connector (all boards)

Pin	Signal Name	Signal Name	Pin
1	n/c	JTAGRST	2
3	JTAGTMS	JTAGTDO	4
5	JTAGTDI	Ground	6
7	Ground	JTAGENL (rev 0)	8
9	n/c	n/c	10
11	BUSMODE2L	VDD (3.3V)	12
13	PCIRSTL	BUSMODE3L	14
15	VDD (3.3V)	BUSMODE4L	16
17	n/c	Ground	18
19	AD30H	AD29H	20
21	Ground	AD26H	22
23	AD24H	VDD (3.3V)	24
25	IDSEL	AD23H	26
27	VDD (3.3V)	AD20H	28
29	AD18H	Ground	30
31	AD16H	C/BE2L	32
33	Ground	n/c	34
35	TRDYL	VDD (3.3V)	36
37	Ground	STOPL	38
39	n/c	Ground	40
41	VDD (3.3V)	n/c	42
43	C/BE1L	Ground	44
45	AD14	AD13H	46
47	M66EN	AD10H	48
49	AD08H	VDD (3.3V)	50
51	AD07H	n/c	52
53	VDD (3.3V)	n/c	54
55	n/c	Ground	56
57	n/c	n/c	58
59	Ground	n/c	60
61	n/c	VDD (3.3V)	62
63	Ground	n/c	64

Note: n/c means no connect – user should not connect to the pin.

3.20.3 Pn4 – Dual LVDS Only

Pin	Signal Name	Signal Name	Pin
1	LVDSA_TX3P	Ground	2
3	LVDSA_TX3N	n/c	4
5	LVDSA_TX2P	Ground	6
7	LVDSA_TX2N	n/c	8
9	LVDSA_TX1P	Ground	10
11	LVDSA_TX1N	n/c	12
13	LVDSA_TX0P	Ground	14
15	LVDSA_TX0N	n/c	16
17	LVDSA_TXCP	Ground	18
19	LVDSA_TXCN	n/c	20
21	LVDSB_TX3P	Ground	22
23	LVDSB_TX3N	n/c	24
25	LVDSB_TX2P	Ground	26
27	LVDSB_TX2N	n/c	28
29	LVDSB_TX1P	Ground	30
31	LVDSB_TX1N	n/c	32
33	LVDSB_TX0P	Ground	34
35	LVDSB_TX0N	n/c	36
37	LVDSB_TXCP	Ground	38
39	LVDSB_TXCN	n/c	40
41	Ground	Ground	42
43	n/c	n/c	44
45	n/c	n/c	46
47	Ground	Ground	48
49	n/c	n/c	50
51	n/c	Ground	52
53	Ground	n/c	54
55	n/c	Ground	56
57	n/c	n/c	58
59	Ground	Ground	60
61	n/c	n/c	62
63	n/c	Ground	64

Note: n/c means no connect – user should not connect to the pin.

3.20.4 Pn4 – Dual LVDS and DVI (In or Out)

Pin	Signal Name	Signal Name	Pin
1	LVDSA_TX3P	Ground	2
3	LVDSA_TX3N	n/c	4
5	LVDSA_TX2P	Ground	6
7	LVDSA_TX2N	n/c	8
9	LVDSA_TX1P	Ground	10
11	LVDSA_TX1N	n/c	12
13	LVDSA_TX0P	Ground	14
15	LVDSA_TX0N	n/c	16
17	LVDSA_TXCP	Ground	18
19	LVDSA_TXCN	n/c	20
21	LVDSB_TX3P	Ground	22
23	LVDSB_TX3N	n/c	24
25	LVDSB_TX2P	Ground	26
27	LVDSB_TX2N	n/c	28
29	LVDSB_TX1P	Ground	30
31	LVDSB_TX1N	n/c	32
33	LVDSB_TX0P	Ground	34
35	LVDSB_TX0N	n/c	36
37	LVDSB_TXCP	Ground	38
39	LVDSB_TXCN	n/c	40
41	Ground	Ground	42
43	DVI_TXCP	n/c	44
45	DVI_TXCN	n/c	46
47	Ground	Ground	48
49	DVI_TX2P	n/c	50
51	DVI_TX2N	Ground	52
53	Ground	n/c	54
55	DVI_TX1P	Ground	56
57	DVI_TX1N	n/c	58
59	Ground	Ground	60
61	DVI_TX0P	n/c	62
63	DVI_TX0N	Ground	64

Note: n/c means no connect – user should not connect to the pin.
DVI = DVID signal set for **DVI In**, DVIB signal set for **DVI Out**

3.20.5 Pn4 - Dual LVDS, DVI (In or Out), Analog Video I/O, VGA

Pin	Signal Name	Signal Name	Pin
1	LVDSA_TX3P	Ground	2
3	LVDSA_TX3N	REAR_ VIN3/HS_HSYNC	4
5	LVDSA_TX2P	Ground	6
7	LVDSA_TX2N	REAR_ VIN2/HS_BLUE	8
9	LVDSA_TX1P	Ground	10
11	LVDSA_TX1N	REAR_ VIN1/HS_GREEN	12
13	LVDSA_TX0P	Ground	14
15	LVDSA_TX0N	REAR_ YIN_VIN0/HS_RED	16
17	LVDSA_TXCP	Ground	18
19	LVDSA_TXCN	REAR_ CIN/HS_VSYNC	20
21	LVDSB_TX3P	Ground	22
23	LVDSB_TX3N	REAR_COUT	24
25	LVDSB_TX2P	Ground	26
27	LVDSB_TX2N	REAR_VOUT	28
29	LVDSB_TX1P	Ground	30
31	LVDSB_TX1N	REAR_YOUT	32
33	LVDSB_TX0P	Ground	34
35	LVDSB_TX0N	REAR_SDA	36
37	LVDSB_TXCP	Ground	38
39	LVDSB_TXCN	REAR_SCL	40
41	Ground	Ground	42
43	DVI_TXCP	REAR_PTC_5V	44
45	DVI_TXCN	REAR_HSYNC	46
47	Ground	Ground	48
49	DVI_TX2P	REAR_VSYNC	50
51	DVI_TX2N	Ground	52
53	Ground	REAR_BLUE	54
55	DVI_TX1P	Ground	56
57	DVI_TX1N	REAR_GREEN	58
59	Ground	Ground	60
61	DVI_TX0P	REAR_RED	62
63	DVI_TX0N	Ground	64

Note: n/c means no connect – user should not connect to the pin.
DVI = DVID signal set for **DVI In**, DVIB signal set for **DVI Out**

3.20.6 Pn4 - Dual LVDS, Dual VGA, Analog Video I/O

Pin	Signal Name	Signal Name	Pin
1	LVDSA_TX3P	Ground	2
3	LVDSA_TX3N	REAR_ VIN3HS_HSYNC	4
5	LVDSA_TX2P	Ground	6
7	LVDSA_TX2N	REAR_ VIN2/HS_BLUE	8
9	LVDSA_TX1P	Ground	10
11	LVDSA_TX1N	REAR_ VIN1/HS_GREEN	12
13	LVDSA_TX0P	Ground	14
15	LVDSA_TX0N	REAR_ YIN_VIN0/HS_RED	16
17	LVDSA_TXCP	Ground	18
19	LVDSA_TXCN	REAR_ CIN/HS_VSYNC	20
21	LVDSB_TX3P	Ground	22
23	LVDSB_TX3N	REAR_COUT	24
25	LVDSB_TX2P	Ground	26
27	LVDSB_TX2N	REAR_VOUT	28
29	LVDSB_TX1P	Ground	30
31	LVDSB_TX1N	REAR_YOUT	32
33	LVDSB_TX0P	Ground	34
35	LVDSB_TX0N	REAR_SDA	36
37	LVDSB_TXCP	Ground	38
39	LVDSB_TXCN	REAR_SCL	40
41	Ground	Ground	42
43	LOCAL_SDA	REAR_PTC_5V	44
45	n/c	REAR_HSYNC	46
47	Ground	Ground	48
49	SO_RED	REAR_VSYNC	50
51	SO_GREEN	Ground	52
53	Ground	REAR_BLUE	54
55	SO_BLUE	Ground	56
57	SO_HSYNC	REAR_GREEN	58
59	Ground	Ground	60
61	SO_VSYNC	REAR_RED	62
63	LOCAL_SCL	Ground	64

Note: n/c means no connect – user should not connect to the pin.

3.20.7 Pn4 - Dual LVDS, VGA, DVI In, DVI Out

Pin	Signal Name	Signal Name	Pin
1	LVDSA_TX3P	Ground	2
3	LVDSA_TX3N	DVI_IN_TX0N	4
5	LVDSA_TX2P	Ground	6
7	LVDSA_TX2N	DVI_IN_TX0P	8
9	LVDSA_TX1P	Ground	10
11	LVDSA_TX1N	DVI_IN_TX1N	12
13	LVDSA_TX0P	Ground	14
15	LVDSA_TX0N	DVI_IN_TX1P	16
17	LVDSA_TXCP	Ground	18
19	LVDSA_TXCN	DVI_IN _TX2P	20
21	LVDSB_TX3P	Ground	22
23	LVDSB_TX3N	DVI_IN _TX2N	24
25	LVDSB_TX2P	Ground	26
27	LVDSB_TX2N	DVI_IN _TXCP	28
29	LVDSB_TX1P	Ground	30
31	LVDSB_TX1N	DVI_IN _TXCN	32
33	LVDSB_TX0P	Ground	34
35	LVDSB_TX0N	REAR_SDA	36
37	LVDSB_TXCP	Ground	38
39	LVDSB_TXCN	REAR_SCL	40
41	Ground	Ground	42
43	DVI_OUT_TXCP	REAR_PTC_5V	44
45	DVI_OUT_TXCN	REAR_HSYNC	46
47	Ground	Ground	48
49	DVI_OUT_TX2P	REAR_VSYNC	50
51	DVI_OUT_TX2N	Ground	52
53	Ground	REAR_BLUE	54
55	DVI_OUT_TX1P	Ground	56
57	DVI_OUT_TX1N	REAR_GREEN	58
59	Ground	Ground	60
61	DVI_OUT_TX0P	REAR_RED	62
63	DVI_OUT_TX0N	Ground	64

Note: n/c means no connect – user should not connect to the pin.

3.20.8 Pn4 - Dual LVDS, Dual VGA, DVI In

Pin	Signal Name	Signal Name	Pin
1	LVDSA_TX3P	Ground	2
3	LVDSA_TX3N	DVI_IN_TX0N	4
5	LVDSA_TX2P	Ground	6
7	LVDSA_TX2N	DVI_IN_TX0P	8
9	LVDSA_TX1P	Ground	10
11	LVDSA_TX1N	DVI_IN_TX1N	12
13	LVDSA_TX0P	Ground	14
15	LVDSA_TX0N	DVI_IN_TX1P	16
17	LVDSA_TXCP	Ground	18
19	LVDSA_TXCN	DVI_IN _TX2P	20
21	LVDSB_TX3P	Ground	22
23	LVDSB_TX3N	DVI_IN _TX2N	24
25	LVDSB_TX2P	Ground	26
27	LVDSB_TX2N	DVI_IN _TXCP	28
29	LVDSB_TX1P	Ground	30
31	LVDSB_TX1N	DVI_IN _TXCN	32
33	LVDSB_TX0P	Ground	34
35	LVDSB_TX0N	REAR_SDA	36
37	LVDSB_TXCP	Ground	38
39	LVDSB_TXCN	REAR_SCL	40
41	Ground	Ground	42
43	LOCAL_SDA	REAR_PTC_5V	44
45	n/c	REAR_HSYNC	46
47	Ground	Ground	48
49	SO_RED	REAR_VSYNC	50
51	SO_GREEN	Ground	52
53	Ground	REAR_BLUE	54
55	SO_BLUE	Ground	56
57	SO_HSYNC	REAR_GREEN	58
59	Ground	Ground	60
61	SO_VSYNC	REAR_RED	62
63	LOCAL_SCL	Ground	64

Note: n/c means no connect – user should not connect to the pin.

3.20.9 Pn4 - Dual LVDS, Single VGA

Pin	Signal Name	Signal Name	Pin
1	LVDSA_TX3P	Ground	2
3	LVDSA_TX3N	n/c	4
5	LVDSA_TX2P	Ground	6
7	LVDSA_TX2N	n/c	8
9	LVDSA_TX1P	Ground	10
11	LVDSA_TX1N	n/c	12
13	LVDSA_TX0P	Ground	14
15	LVDSA_TX0N	n/c	16
17	LVDSA_TXCP	Ground	18
19	LVDSA_TXCN	n/c	20
21	LVDSB_TX3P	Ground	22
23	LVDSB_TX3N	n/c	24
25	LVDSB_TX2P	Ground	26
27	LVDSB_TX2N	n/c	28
29	LVDSB_TX1P	Ground	30
31	LVDSB_TX1N	n/c	32
33	LVDSB_TX0P	Ground	34
35	LVDSB_TX0N	REAR_SDA	36
37	LVDSB_TXCP	Ground	38
39	LVDSB_TXCN	REAR_SCL	40
41	Ground	Ground	42
43	n/c	REAR_PTC_5V	44
45	n/c	REAR_HSYNC	46
47	Ground	Ground	48
49	n/c	REAR_VSYNC	50
51	n/c	Ground	52
53	Ground	REAR_BLUE	54
55	n/c	Ground	56
57	n/c	REAR_GREEN	58
59	Ground	Ground	60
61	n/c	REAR_RED	62
63	n/c	Ground	64

Note: n/c means no connect – user should not connect to the pin.

3.20.10 Pn4 – RG-101 Compatible VGA Pinout

Pin	Signal Name	Signal Name	Pin
1	n/c	Ground	2
3	n/c	n/c	4
5	n/c	Ground	6
7	n/c	n/c	8
9	n/c	Ground	10
11	n/c	n/c	12
13	n/c	Ground	14
15	n/c	n/c	16
17	n/c	Ground	18
19	n/c	n/c	20
21	n/c	Ground	22
23	n/c	n/c	24
25	n/c	Ground	26
27	n/c	n/c	28
29	n/c	Ground	30
31	n/c	n/c	32
33	n/c	Ground	34
35	n/c	n/c	36
37	n/c	Ground	38
39	n/c	n/c	40
41	Ground	Ground	42
43	REAR_HSYNC	REAR_VSYNC	44
45	Ground	REAR_RED	46
47	REAR_GREEN	REAR_BLUE	48
49	n/c	n/c	50
51	n/c	Ground	52
53	Ground	n/c	54
55	n/c	Ground	56
57	n/c	n/c	58
59	Ground	Ground	60
61	n/c	n/c	62
63	n/c	Ground	64

Note: n/c means no connect – user should not connect to the pin.

Chapter 4
Installing Your Rastergraf Graphics Board

4.1 Introduction

There are 2 steps involved in getting your Rastergraf board to work in your system:

- Unpack and install the Rastergraf board.
- Install the software

This chapter shows you how to install the Rastergraf board in your computer. Your Rastergraf software User's Manual (e.g., SDL) provides instructions on how to install the software.

4.2 Unpacking Your Board

When you unpack your board, inspect the contents to see if any damage occurred in shipping. If there has been physical damage, file a claim with the carrier at once and contact Rastergraf for information regarding repair or replacement. Do not attempt to use damaged equipment.

> **Caution**
>
> Be careful not to remove the board from its antistatic bag until you are ready to install it. It is preferable to wear a grounded wrist strap whenever handling computer boards.

Some operating systems require that you reboot your system after installing a device driver, because only after the reboot will your system utilize the driver and recognize the board. If yours is such an operating system, you might like to install your Rastergraf software **before** installing the board since you will have to shut down the computer to install the board anyway. If you want to install the software before shutting down the computer, proceed to the correct part of the relevant software manual and return to this chapter afterwards.

4.3 Preparing for Installation

The Topaz, Stratus, Tropos, Garnet, and Duros are PMC boards. However, they can be installed in PCI and CompactPCI backplanes by using an appropriate bus adapter (see Section 4.4, Important Compatibility Note). In order to ease the procedure, there follows individual sections that deal with each board type.

4.3.1 Interrupt Settings

The boards use the PMC **INTA** interrupt request line for the particular slot it is plugged into. In some computers, each slot ***may*** map its local interrupt lines to a permuted set of INTA-INTD, which means that the board will show up on a different interrupt line according to the slot it is plugged into. The device driver will usually notice this and compensate for it. In any case, the user has no direct control (e.g., jumpers) over what interrupt line the graphics board will use.

4.3.2 Address Settings

Since the PCI bus and the boards are configured by the Operating System (OS) and/or BIOS while booting up, there aren't any address jumpers. The address settings are programmable and are set up by the software as a result of information supplied by the OS at boot time. Refer to the Rastergraf software User's Manuals for more information.

The software sets up the BARs (Base Address Registers) and other relevant control registers in all of the PCI devices on the board. The Rastergraf device drivers will load the BARs if the OS or BIOS did not. If you can determine the actual PCI base address, you might even be able to probe the address spaces with an on-line debugger once the driver code has run. The SM731 Data Book has detailed information on how it controls access to the on-board registers.

The ability to probe the board is dependent on the CPU memory map as implemented by the system OS and the address ranges of the PCI bus as determined by the CPU hardware. These things change from OS to OS, board-to-board, and vendor-to-vendor, making it a difficult task. Most likely, if you use Rastergraf supplied software, the board will show up and you will get pictures.

4.3.3 Changing the Jumpers

In the following subsections, please refer ***Figures 4-1, 4-2,*** and ***4-3.***

JP1: VGA PCI Device Jumper

JP1 enables SM731 VGA BIOS to respond. If you are running in a PC compatible machine and you want some other graphics board to run as console, you may need to remove this jumper. This will prevent the system BIOS from loading a VGA BIOS from the Rastergraf board.

> **Note:**
>
> The Rastergraf Windows 2K/XP driver does not usually work well in concert with a different kind of graphics board. In other words, if you need to have two graphics boards in the system, they both (or neither) have to be Rastergraf boards.
>
> If your CPU chip set has a built-in graphics adapter and you want to run Windows, you have to disable it in the system BIOS prior to installing the Rastergraf board.

JP2 and JP4: Alternate BIOS Image Jumpers 0 and 1

These jumpers are installed to select alternate BIOS images. At present, these jumpers are not used.

JP3: Local 3.3V Regulator Enable

If the graphics board was built with the optional local 3.3V regulator (VR1), ***install*** JP3 to enable the regulator to supply 3.3V power to the graphics board when the PMC backplane only has 5V.

Figure 4-1 Jumper Locations for the Fab Rev 0 TopazPMC Board

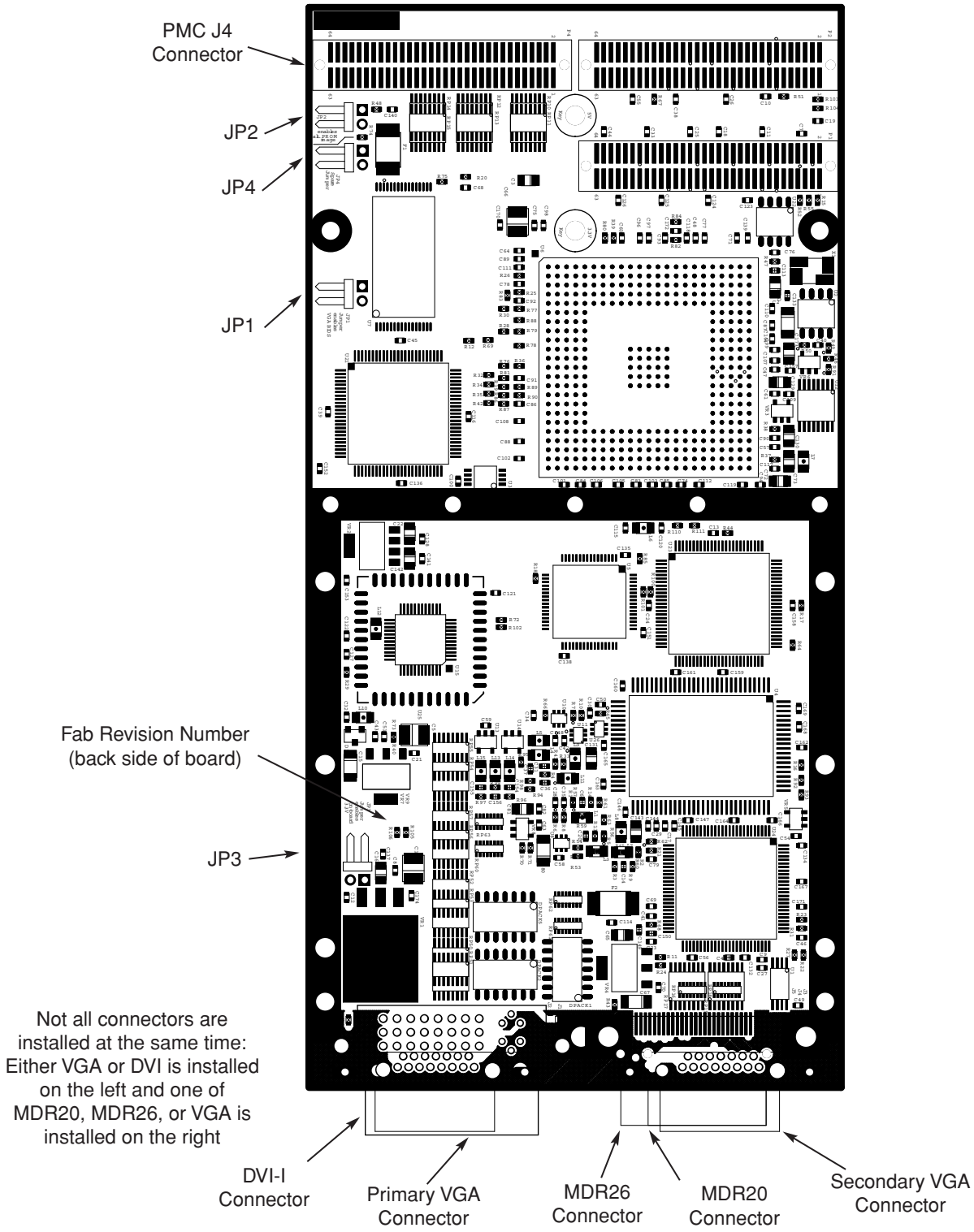


Figure 4-2 Jumper Locations for the Fab Rev 1 TopazPMC Board

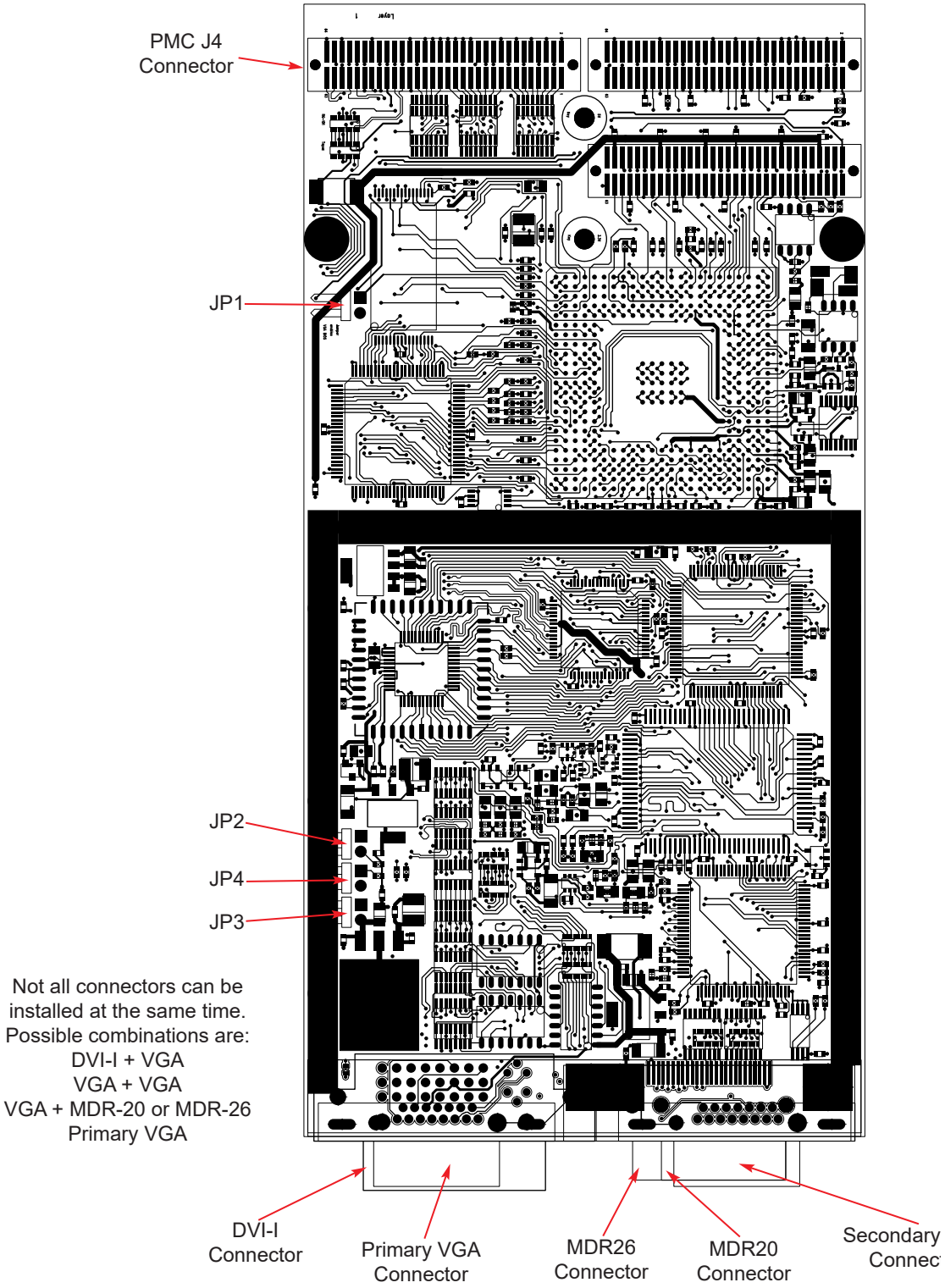


Figure 4-3 Jumper Locations for the Fab Rev 2 TopazPMC Board

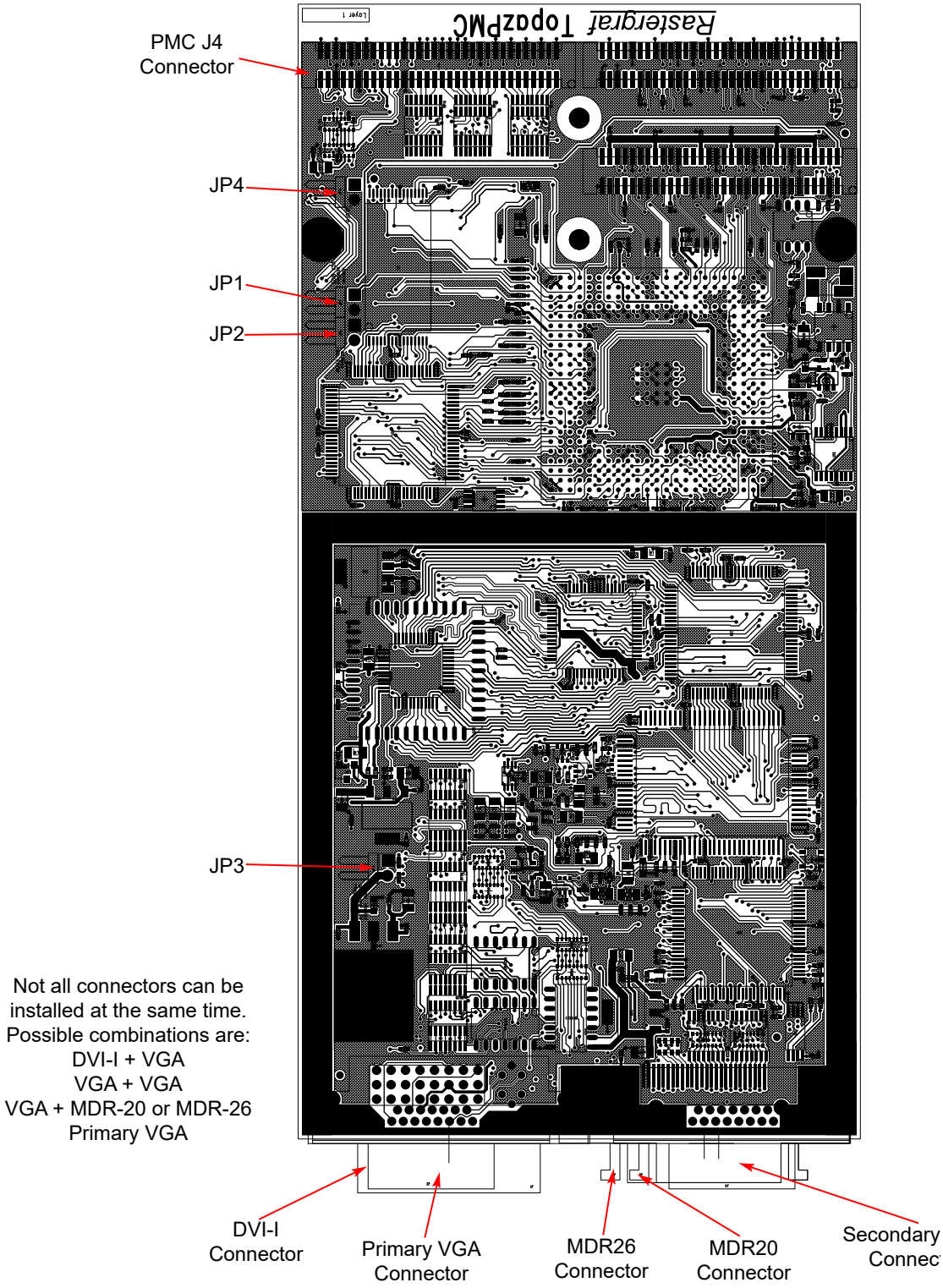


Figure 4-4 Jumper Locations for the Fab Rev 1 StratusPMC and TroposPMC Boards

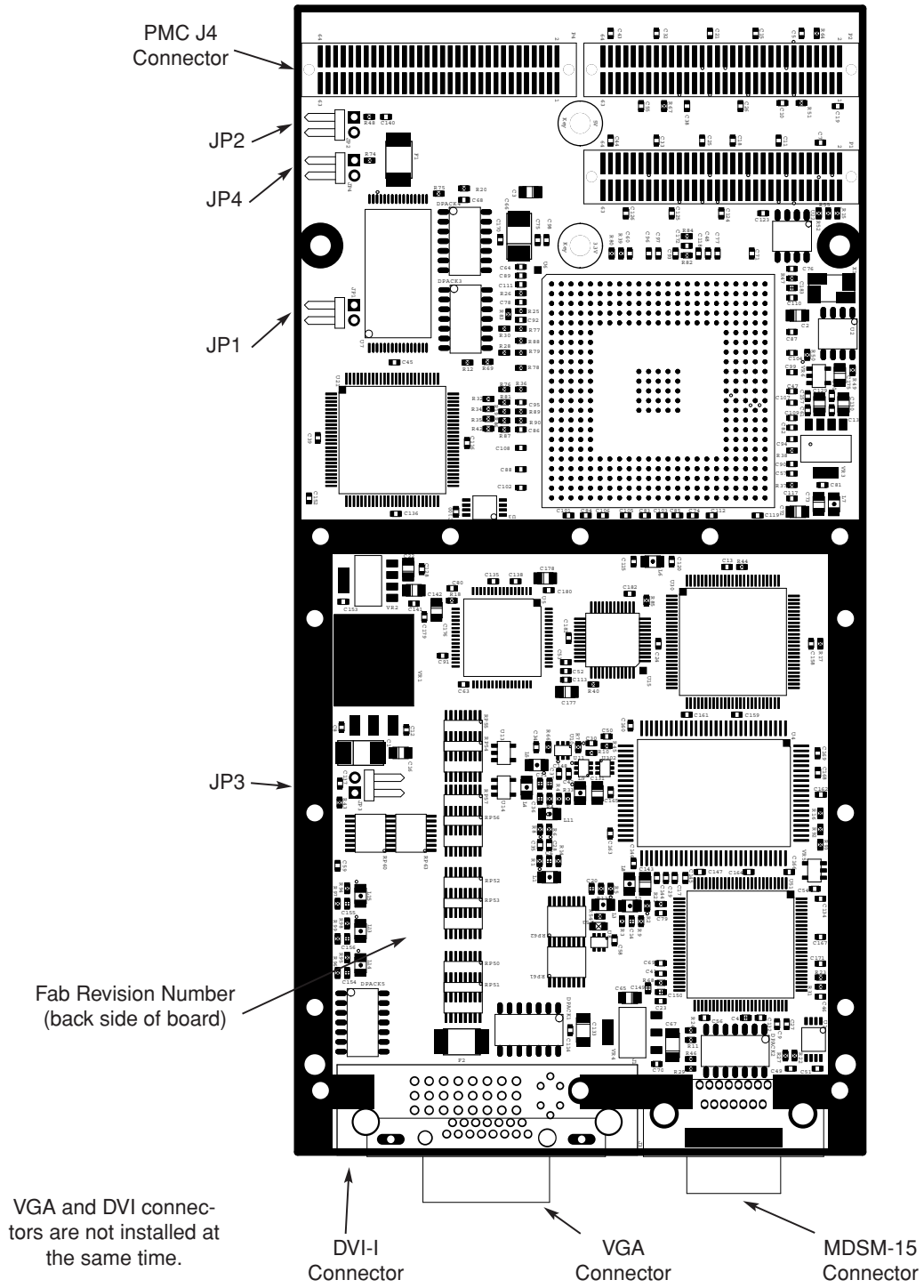
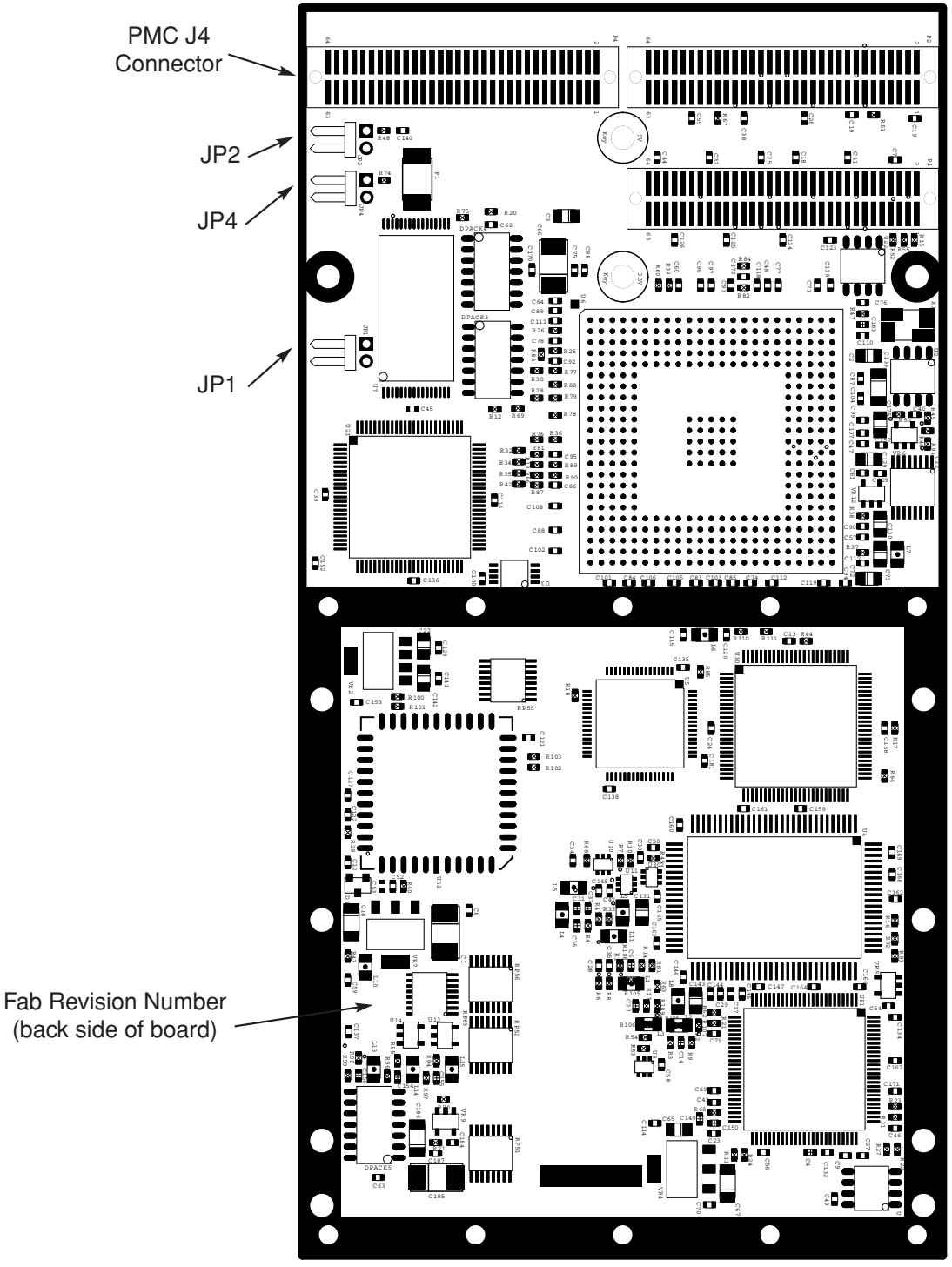


Figure 4-5 Jumper Locations for the Fab Rev 1 Garnet and Duros Boards



4.4 Graphics Board Installation

The graphics board can plug into any 32-bit, 33 or 66 MHz, 5V or 3.3V signaling IEEE 1386-2001 compatible single module PMC location. Such locations are most commonly found on VME and CompactPCI computers.

The graphics will also work in CompactPCI or PCI systems by using a carrier.

Important Compatibility Note:

While the graphics boards will work in a PCI or CompactPCI passive (no on-board bridge) carriers, the timing margins of the SM731 are such that the graphics boards will not work reliably at 66 MHz.

Unless you are certain that your system is running and will always be run only at 33 MHz, you must use an active (on-board bridge) PCI or CompactPCI carrier.

	33 MHz	66 MHz	See
CompactPCI	Active or passive	Active (on-board bridge)	Section 4.6
PCI	Active or passive	Active (on-board bridge)	Section 4.5

Note:

Older VME host or carrier boards may not supply 3.3V to the PMC connectors. The graphics board requires both 3.3V and 5V. It will not operate correctly in any system that does not supply BOTH 5V and 3.3V.

By special order, Rastergraf can supply the Topaz, Stratus, and Tropos graphics boards with a local 3.3V regulator installed. Garnet and Duros boards do not have a local regulator option. Please contact Rastergraf for assistance.

Installation Procedure

Note:

Refer to ***Section 4.3.3*** for the settings for JP1 – JP4.

1. Shut down the operating system and **turn off the power**.

Warning!

Never open the computer without turning off the power supply. Unless internal AC wiring is exposed, leave the power cord plugged in, so as to ground the computer chassis. You can easily get shocked, ruin computer parts or both unless you turn off the power. Even with power switched off, lethal voltages can exist in the equipment.

2. Open the computer and remove the CPU board onto which the graphics PMC board is to be installed. Identify an empty PMC location (generally there are one or two on a given CPU board). The graphics PMC board is a Universal PMC/PCI device and can be plugged into a PMC port which uses either 5V or 3.3V signaling.

   THE CARRIER MUST SUPPLY BOTH 3.3V AND 5V unless the graphics board has a local 3.3V regulator installed.

3. Take care to optimize airflow by blocking off unused slots in the card cage, and arrange the boards to permit optimum airflow through them.

Caution

The static electricity that your body builds up normally can seriously damage the components on the graphics board.

Figure 4-6 Installation of a PMC Module into an Emerson MVME2604

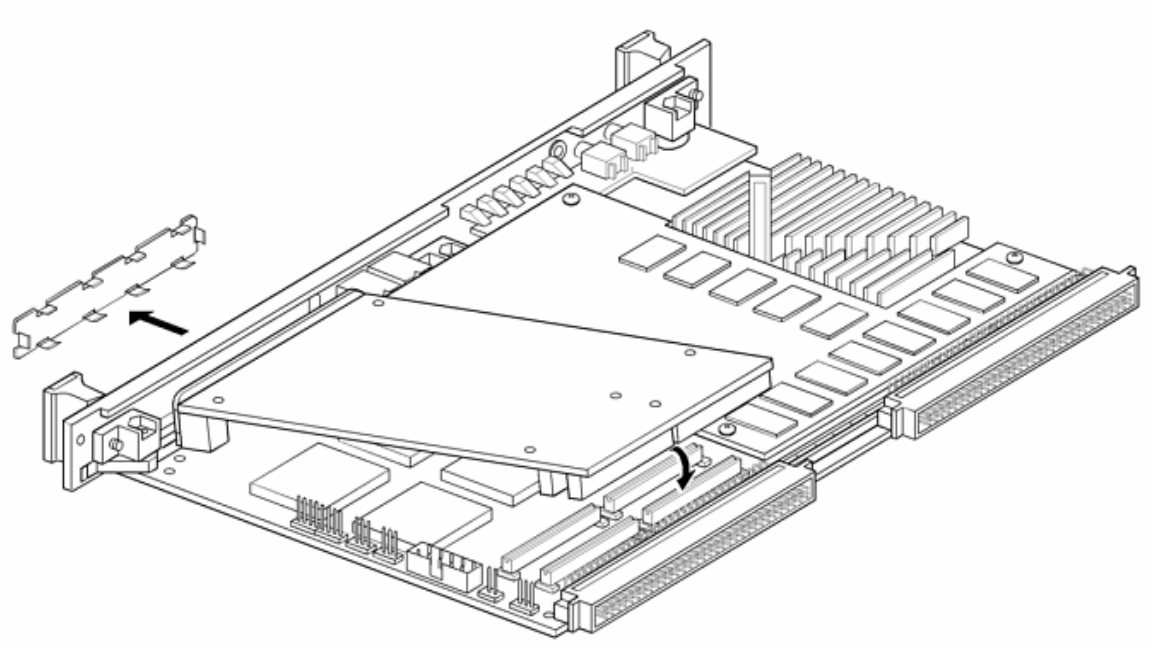
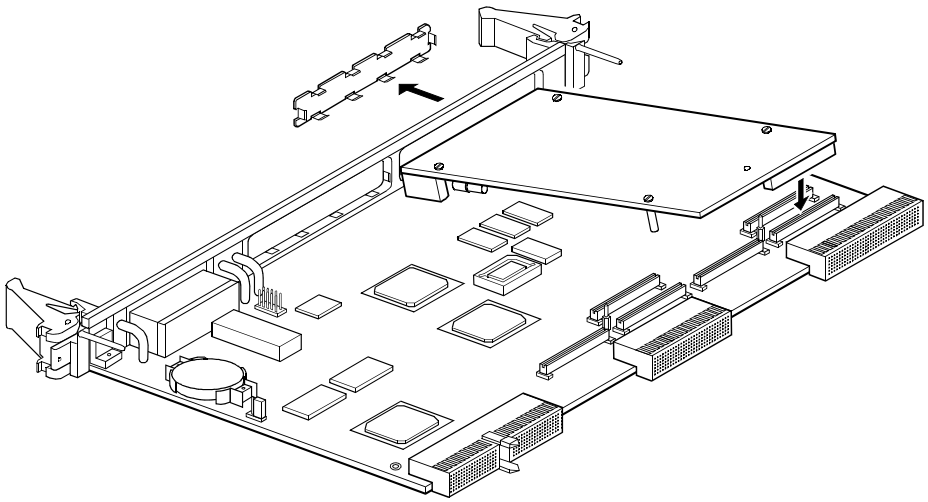


Figure 4-7 Installation of the PMC Module into an Emerson CPV3060



4. Touch a metal part of the computer chassis, remove the graphics board from its anti static bag, and immediately slip it into the slot. After ensuring that the board is seated correctly, install the mounting screws (two near the front and two near the PMC connectors).

Note

Sometimes the graphics board front panel can hang up going into the carrier front panel hole. This can be because there is a little rubber EMI gasket that is installed in a slot cut into the graphics board front panel. If the hole in the carrier board is “on the small side” it can be difficult if not impossible to install the graphics board. In this case, you will have to remove and discard the gasket.

5. Close the computer.

Now, go to Section 4.7.

4.5 Installing in a PCI Backplane using a Carrier

You can install a graphics board into a PCI computer if you first plug it into a PMC-to-PCI adapter board (see Section 4.4, Important Compatibility Note). The adapters are designed to plug into any standard PCI 2.2 specification compatible backplane.

Note:

Most AT style motherboards do not supply 3.3V to the PCI connectors. If the computer is listed as PCI 2.0 or 2.1 compliant, it probably does not supply 3.3V. Since most carriers have an on-board 3.3V regulator, this should not be a problem. Make sure that the carrier is correctly configured to supply local 3.3V.

Installation Procedure

1. Shut down the operating system and **turn off the power**.

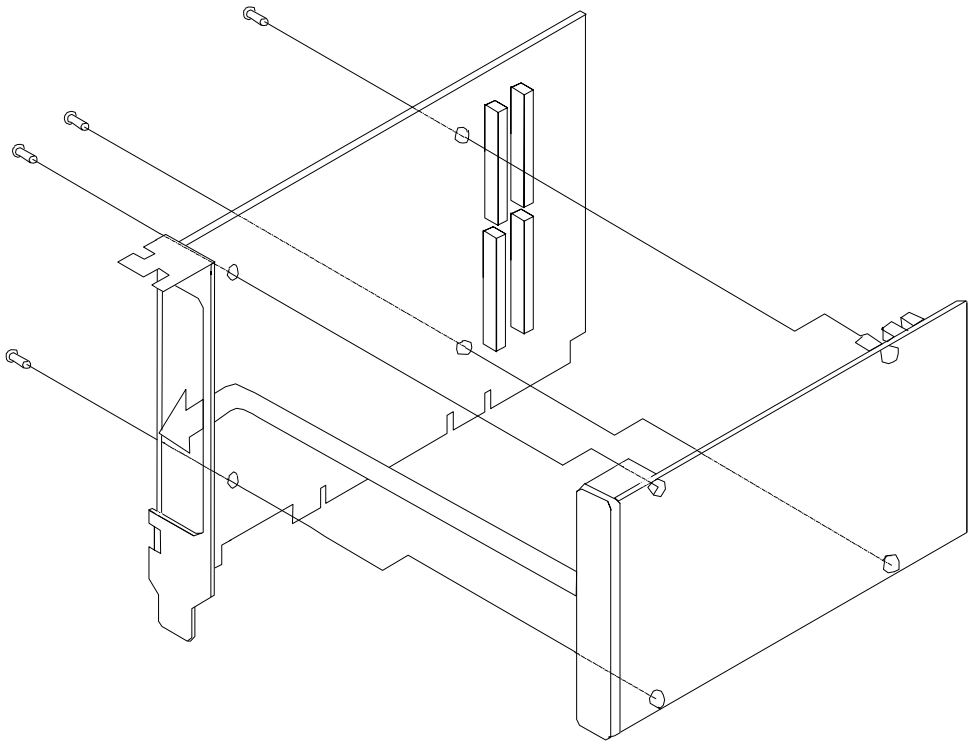
Warning!

Never open the computer without turning off the power supply. Unless internal AC wiring is exposed, leave the power cord plugged in, so as to ground the computer chassis. You can easily get shocked, ruin computer parts or both unless you turn off the power. Even with power switched off, lethal voltages can exist in the equipment.

2. Open the computer and find an empty PCI slot.

   The graphics boards are Universal PCI devices and can be plugged into a position which uses either 5V or 3.3V signaling protocol. If you use a 32-bit/64-bit carrier, note that when used with a Topaz, Stratus, Tropos, Garnet, or Duros, the carrier's high 32 bits are not connected.

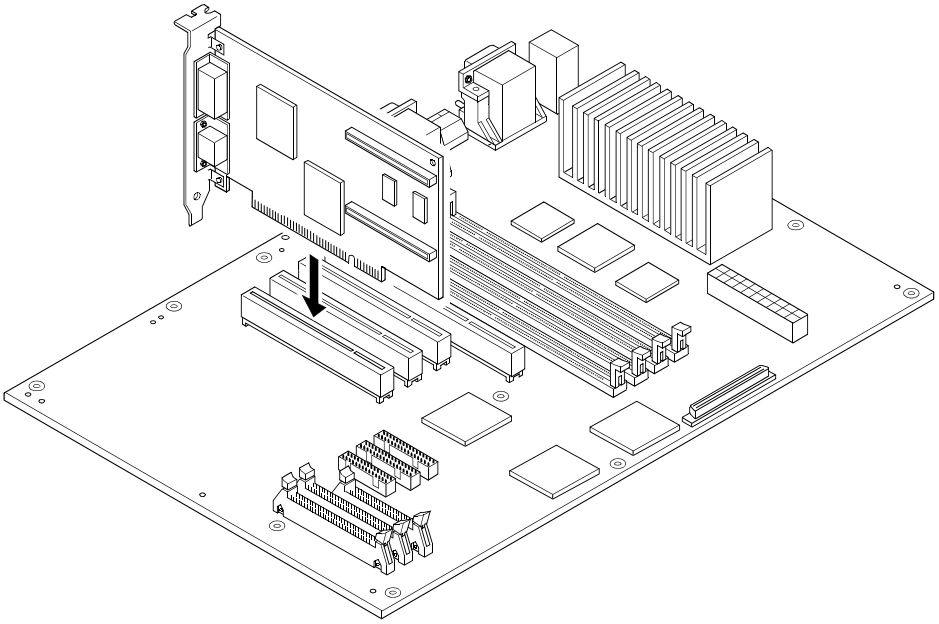
Figure 4-8 Installation of a PMC Module onto a PCI-PMC Carrier



Caution
The static electricity that your body builds up normally can seriously damage the components on the graphics board.

3. Wear a grounded wrist strap and touch a metal part of the computer chassis. Remove the card slot blocking plate from the chassis. Then, remove the graphics board from its anti static bag, and immediately slide it into the slot.

Figure 4-9 Installation of a PCI Module into an Emerson MTX



4. After making sure the board is seated correctly, install the screw into the place where the blocking plate was and which (now) holds the graphics board's front panel
5. Close the computer.

Now, go to Section 4.7.

4.6 Installing in a CompactPCI Backplane using a Carrier

You can install a graphics board into a CompactPCI computer if you first plug it into a PMC-to-CompactPCI adapter board (see Section 4.4, Important Compatibility Note).

Installation Procedure

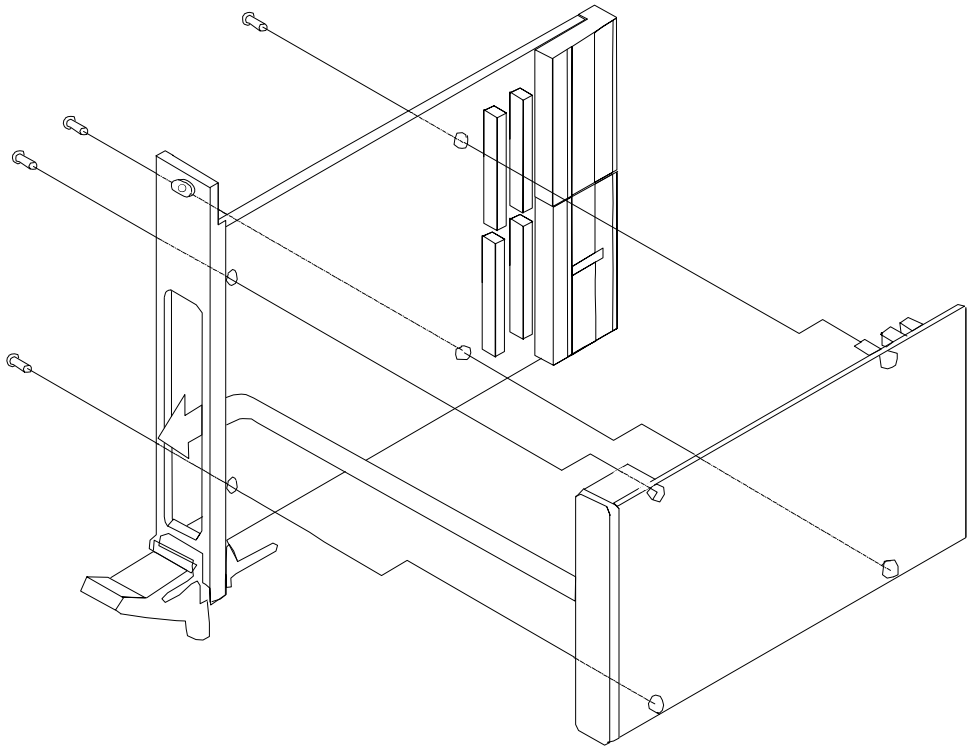
1. Shut down the operating system and **turn off the power**.

> **Warning!**
>
> Never open the computer without turning off the power supply. Unless internal AC wiring is exposed, leave the power cord plugged in, so as to ground the computer chassis. You can easily get shocked, ruin computer parts or both unless you turn off the power. Even with power switched off, lethal voltages can exist in the equipment.

2. Open the computer and identify the empty slot in the card cage that is closest to the CPU. Do not leave any slots empty between the graphics board and the CPU.

   The graphics boards are Universal PCI devices and can be plugged into a position which uses either 5V or 3.3V signaling protocol. Therefore, a CompactPCI J1 connector signaling key plug is not necessary. Note that when used with a Topaz, Stratus, Tropos, Garnet, or Duros, the carrier's high 32 bits are not connected.

Figure 4-10 Installation of a PMC Module onto a 3U CPCI- PMC Carrier



Caution

The static electricity that your body builds up normally can seriously damage the components on the graphics board.

3. Wear a grounded wrist strap. Touch a metal part of the computer chassis, remove the graphics board from its anti static bag, and immediately slide it into the slot.

Figure 4-11 Installation of a PMC Module into a 6U CPCI- PMC Carrier

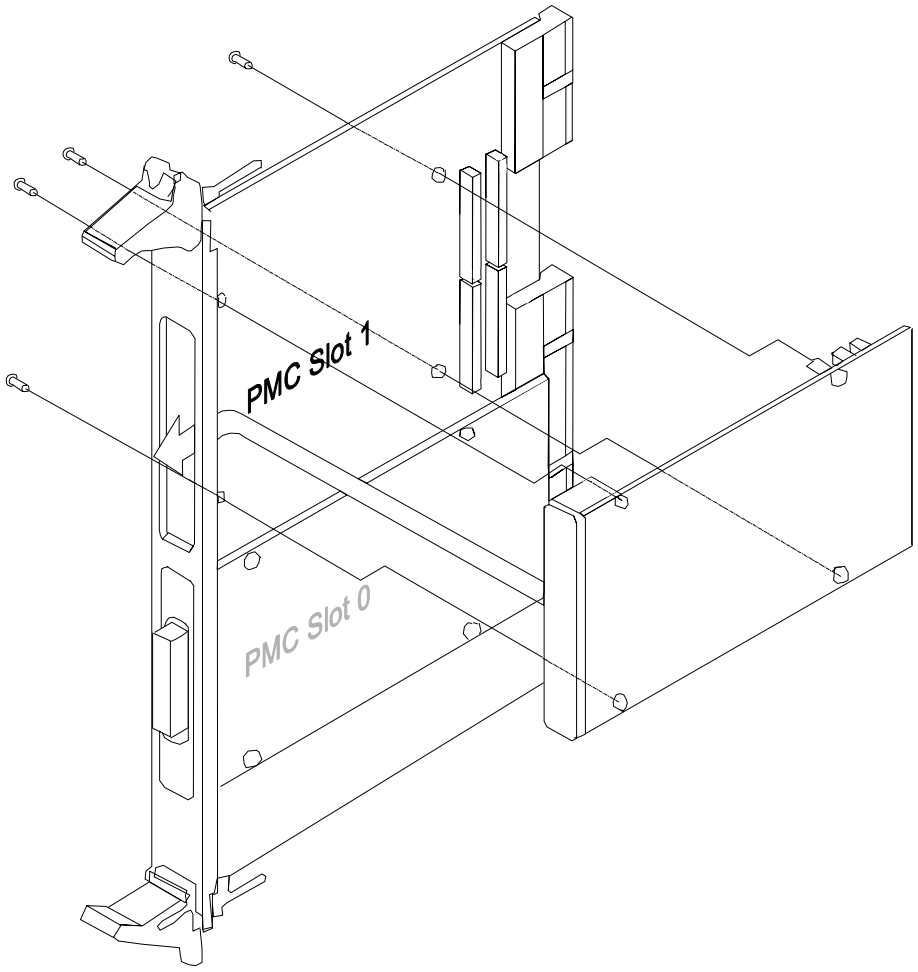
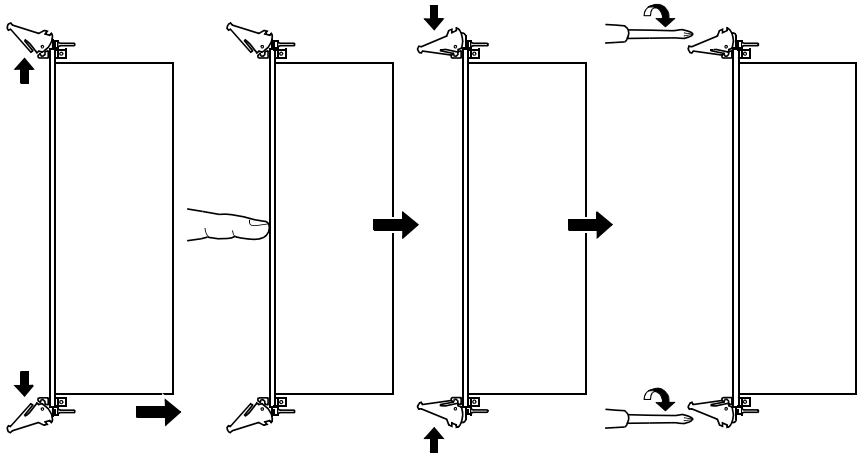


Figure 4-12 Installing a CompactPCI Board



4. After making sure the board is seated correctly, lever the card in with the injector(s) and tighten the screwlock on each end of the faceplate.

Now, go to Section 4.7.

4.7 Finishing the Installation

4.7.1 Connecting to the Monitor

Be sure to snug the connector's thumbscrews down, as it may otherwise work loose and cause unreliable operation.

Connecting to the Pn4

Note that because of the specialized nature of the work, Rastergraf does not supply standard cables or any adapters for use with boards with Pn4 (rear panel) connections. You are on your own for cabling.

Connecting to the TopazPMC/1V or TroposPMC/1V

If you have a non-DVI capable TopazPMC/1V or TroposPMC/1V board, you can plug VGA cable(s) directly into the VGA compatible front panel connector(s).

> **Note**
>
> Because two VGA connectors are a tight fit on a PMC board, some VGA cable connector moldings are too wide to allow two cables to be plugged in simultaneously on the GeminiPMC/1. Rastergraf can supply cables that are known to fit. Please see Section 3.8.

Connecting to the TroposPMC/1V

If you have a TroposPMC/2 (with DVI), plug your DVI monitor cable into the DVI-I connector on the front panel. If you wish to use VGA instead, plug a DVI-VGA adapter into the Tropos DVI connector and connect the other end to the VGA cable.

Connecting to the TopazPMC/1L

If you have a TopazPMC/1L (LVDS), you can plug a VGA monitor cable into the VGA connector on the front panel. Alternatively, and more likely, you can connect one or two LVDS panels to the MDR26 connector using a custom or standard cable (see Chapter 3).

Connecting to a TopazPMC/2x or StratusPMC/2x

If you have a DVI-capable Topaz or Stratus and wish only to use the DVI monitor, plug your DVI monitor cable into the DVI-I connector on the front panel. If you wish to use only the primary VGA instead, plug a DVI-VGA adapter into the DVI connector and connect the other end to the VGA cable.

If you wish use some combination of VGAs and DVI, then use the DVI-I Breakout cable to connect to DVI or the VGA channels.

4.7.2 Checking your Display

Note

The boards can supply 3 Wire (RGB with sync on green, BNC connectors) or 5 Wire Video (RGBHV, VGA connector). Rastergraf software defaults to 5 Wire Video (NO sync on green).

Be aware that if you connect a board that has video parameters set up for sync on green to a VGA compatible monitor you will get a green background on the display.

This is an interesting problem. If you have a Sun SPARC or PC, the BIOS firmware in the graphics board will be invoked and you will get some sort of display on power-up.

But, if you have a PowerPC system running VxWorks, you will not get any visual indication that the board is operational until you load and run some graphics board-specific software like SDL or X Windows.

If you have such a system and are ever in doubt about whether the board really works, you would be well advised to plug it into a PMC to PCI carrier and plug it into a PC to try it out.

Please proceed to the next section.

4.8 Using a Rastergraf Board in a PC

> **Note:**
>
> The Rastergraf Windows 2K/XP driver does not usually work well in concert with a different kind of graphics board. In other words, if you need to have two graphics boards in the system, they both (or neither) have to be Rastergraf boards.
>
> If your CPU chip set has a built-in graphics adapter and you want to run Windows, you have to disable it in the system BIOS prior to installing the Rastergraf board.

4.8.1 Single Graphics Board

If you are using a PC and the Rastergraf board is to be the system display (and you don't have another VGA controller installed), the system BIOS should find the Rastergraf board, and initialize the display.

4.8.2 Multiboard Operation

The Windows 2K/XP drivers, Linux and VxWorks SDL, and XFree86 4.3 support multihead operation.

If you have another Rastergraf VGA board in the system, the order in which the boards are plugged into the backplane or motherboard will determine which board will be used for the system display. If the BIOS picks the wrong one, turn off the computer and swap the boards' positions.

If your system has a non-removable VGA controller and you want to use the Rastergraf board as the system display you may have a problem. If the BIOS starts up using the built-in VGA, you may be able to disable it with a BIOS setting. Otherwise, contact the system board manufacturer. Failing these things, you are probably out of luck.

Table 4-1 x86 Supported Video Modes

Standard IBM Compatible VGA Modes

The table details the standard VGA modes supported in CRT only.

Table 1: **Standard IBM Compatible VGA Modes**

Mode # (Hex)	Type	Colors	Alpha	Resolution	Font	Clock MHz	Hsync KHz	Vsync Hz	Memory Min	Buffer Start
0,1	Txt	16	40x25	320x200	8x8	25.175	31.55	70.3	256K	B8000
0,1*	Txt	16	40x25	320x350	8x14	25.175	31.55	70.3	256K	B8000
0,1+	Txt	16	40x25	360x400	9x16	28.322	31.34	69.8	256K	B8000
2,3	Txt	16	80x25	640x200	8x8	25.175	31.55	70.3	256K	B8000
2,3*	Txt	16	80x25	640x350	8x14	25.175	31.55	70.3	256K	B8000
2,3+	Txt	16	80x25	720x400	9x16	28.322	31.34	69.8	256K	B8000
4,5	Gr	4	40x25	320x200	8x8	25.175	31.55	70.3	256K	B8000
6	Gr	2	80x25	640x200	8x8	25.175	31.55	70.3	256K	B8000
7	Txt	Mono	80x25	720x350	9x14	28.322	31.34	69.8	256K	B8000
7+	Txt	Mono	80x25	720x400	9x16	28.322	31.34	69.8	256K	B8000
D	Gr	16	40x25	320x200	8x8	25.175	31.55	70.3	256K	A0000
E	Gr	16	80x25	640x200	8x8	25.175	31.55	70.3	256K	A0000
F	Gr	Mono	80x25	640x350	8x14	25.175	31.55	70.3	256K	A0000
10	Gr	16	80x25	640x350	8x14	25.175	31.55	70.3	256K	A0000
11	Gr	2	80x30	640x480	8x16	25.175	31.55	60.1	256K	A0000
12	Gr	16	80x30	640x480	8x16	25.175	31.55	60.1	256K	A0000
13	Gr	256	40x25	320x200	8x8	25.175	31.55	70.3	256K	A0000

NOTE: For Modes 3 and 7, 8-dot Fonts are used on the LCD.

VESA Super VGA Modes

VESA extended video modes are supported by the LYNX family BIOS (subject to the constraints of the video subsystem hardware) as follows:

Table 2: **VESA Super VGA Modes**

VESA Mode # (Hex)	Extended Mode	Type	Colors	Alpha	Resolution	Font	Memory Min	Buffer Start
(Min.)	Buffer Start							
101	50	Gr	256	80x30	640x480	8x16	512K	A0000
102	6A	Gr	16	100x75	800x600	8x8	256K	A0000
103	55	Gr	256	100x75	800x600	8x8	512K	A0000
104	6B	Gr	16	128x48	1024x768	8x16	512K	A0000
105	60	Gr	256	128x48	1024x768	8x16	1M	A0000
107	65	Gr	256	160x64	1280x1024	8x16	2M	A0000
111	52	Gr	64K	80x30	640x480	8x16	1M	A0000
112	53	Gr	16M	80x30	640x480	8x16	1M	A0000
114	57	Gr	64K	100x75	800x600	8x8	1M	A0000
115	58	Gr	16M	100x75	800x600	8x8	2M	A0000
117	62	Gr	64K	128x100	1024x768	8x8	2M	A0000
118	63	Gr	16M	128x100	1024x768	8x8	4M	A0000
11A	67	Gr	64K	160x128	1280x1024	8x8	4M	A0000
11B	68	Gr	16M	160x128	1280x1024	8x8	4M	A0000

Table 4-1 x86 Supported Video Modes (continued)

Low Resolution Modes

The BIOS supports low-resolution modes from 320x200 to 640x400 in 8/16-bit colors for DirectDraw. The low resolution modes are defined as follows:

Table 3: **Low Resolution Modes**

Mode # (Hex)	Type	Colors	Resolutions	Vsync (Hz)	Video Memory	Buffer Start
40	Gr	256	320x200	70	1MB	A0000
41	Gr	64K	320x200	70	1MB	A0000
42	Gr	256	320x240	75, 60	1MB	A0000
43	Gr	64K	320x240	75, 60	1MB	A0000
44	Gr	256	400x300	75, 60	1MB	A0000
45	Gr	64K	400x300	75, 60	1MB	A0000
46	Gr	256	512x384	75	1MB	A0000
47	Gr	64K	512x384	75	1MB	A0000
48	Gr	256	640x400	70	1MB	A0000
49	Gr	64K	640x400	70	1MB	A0000

NOTE: For modes 320x240 and 400x300, default refresh rate is set to 60Hz and optimal is set to 75Hz.

640 by 480 Resolution Modes

Table 4: **640 x 480 Extended Modes**

Mode # (Hex)	VESA Mode # (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
50	101	Gr	256	80x30	8x16	25.175	31.5	60.0	512 KB	A0000
						31.5	37.5-	75.0-		
						36	43.3	85.0		
52	111	Gr	64K	80x30	8x16	25.0	31.5	60.0	1MB	A0000
						31.5	37.5-	75.0-		
						36	43.3	85.0		
53	112	Gr	16M (24-bit)	80x30	8x16	25.0	31.5	60.0	1MB	A0000
						31.5	37.5-	75.0-		
						36	43.3	85.0		
54		Gr	16M (32-bit)	80x30	8x16	25.0	31.5	60.0	2MB	A0000
						31.5	37.5-	75.0-		
						36	43.3	85.0		

NOTE: For the above resolutions, the default refresh rate for LCD and Simul mode is 60Hz.

Table 4-1 x86 Supported Video Modes (continued)

800 by 600 Resolution Modes

Table 5: **800x600 Extended Modes**

Mode # (Hex)	Vesa Mode# (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
6A	6A	Gr	16	100x75	8x8	40.0	37.9+	60.3+	256KB	A0000
55	103	Gr	256	100x75	8x8	40.0	37.9+	60.3+	512KB	A0000
						49.5	46.9+	75.0+		
						56.25	53.7	85.0		
57	114	Gr	64K	100X75	8X8	40.0	37.9+	60.3+	1MB	A0000
						49.5	46.9+	75.0+		
						56.25	53.7	85.0		
58	115	Gr	16M (24-bit)	100X75	8X8	40.0	37.9+	60.3+	2MB	A0000
						49.5	46.9+	75.0+		
						56.25	53.7	85.0		
59		Gr	16M (32-bit)	100X75	8X8	40.0	37.9+	60.3+	2MB	A0000
						49.5	46.9+	75.0+		
						56.25	53.7	85.0		

NOTE: For the above resolutions, the default refresh rate for LCD and Simul mode is 60Hz.

1024 by 768 Resolution Modes

Table 6: **1024x768 Extended Modes**

Mode # (Hex)	VESA Mode# (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
6B	104	Gr	16	128x48	8x16	65.0	48.4 -	60.0 -	512KB	A0000
60	105	Gr	256	128x48	8x16	65.0	48.4 -	60.0 -	1MB	A0000
						78.8	60.0+	75.0+		
						94.5	68.7	85.0		
62	117	Gr	64K	128x48	8x16	65.0	48.4 -	60.0 -	2MB	A0000
						78.8	60.0+	75.0+		
						94.5	68.7	85.0		
63	118	Gr	16M (24-bit)	128x48	8x16	65.0	48.4 -	60.0 -	4MB	A0000
						78.8	60.0+	75.0+		
						94.5	68.7	85.0		
64		Gr	16M (32-bit)	128x48	8x16	65.0	48.4 -	60.0 -	4MB	A0000
						78.8	60.0+	75.0+		
						94.5	68.7	85.0		

NOTE: For the above resolutions, the default refresh rate for LCD and Simul mode is 60Hz

Table 4-1 x86 Supported Video Modes (continued)

Table 7: **1280x1024 Extended Modes**

Mode # (Hex)	VESA Mode# (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
65	107	Gr	256	160x64	8x16	78.8	46.4	86.8i+	2 MB	A0000
						108	64	60.0		
						135	79.98	75.0		
67	11A	Gr	64K	160x64	8x16	78.8	46.4	86.8i+	4 MB	A0000
						108	64	60.0		
						135	79.98	75.0		
68		Gr	16M (24-bit)	160x64	8x16	78.8	46.4	86.8i+	4 MB	A0000
						108	64	60.0		
						135	79.98	75.0		

NOTE: For the above resolutions, the default refresh rate for LCD and Simul mode is 60Hz

1600 by 1200 Resolution Modes

Table 8: **1600x1200 Extended Modes**

Mode # (Hex)	VESA Mode# (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
70		Gr	256	200x75	8x16	162	74.5	60	2 MB	A0000
						202	84	75		
						229	91.8	85		
72		Gr	64K	200x75	8x16	112	74.5	60	4 MB	A0000
						202	84	75		
						229	91.8	85		

4.9 Using a Rastergraf Board in a PowerPC

If the CPU's on-board firmware is VGA aware, it should initialize the graphics board and use it as the system console. However, many PowerPC (PPC) based computers don't have generic VGA support. Your best bet is to use a board with a VGA BIOS in it.

Otherwise, you will have to boot using a serial terminal and only after the graphics software has been installed and run will you see anything.

4.10 Final Checks

If you are running in a PC, then you should get the usual PC displays. If you have multiple graphics boards installed, only one will be initialized by the BIOS. Once you have installed the Windows 2K/XP multihead drivers and reboot, all screens will be initialized as the OS boots.

In the case of X Windows, your monitor should display a uniform stippled raster and a cross-hair cursor, which is controlled by the mouse. If you have multiple graphics boards installed, all screens will be initialized and display the stipple once you have the server installed and running.

For SDL, demo programs are provided that may be run to put test patterns on the screen(s).

Pictures!

Once you have a picture on the screen, you may need to adjust the width, height, brightness, contrast, and hold controls on your monitor to get a good, centered image. If these controls don’t adjust the image properly, the parameters used to set the graphics timing registers might be wrong. If you have any trouble with any part of the installation call or email Rastergraf for assistance, or refer to Chapter 6.

Chapter 5 Programming On-board Devices and Memories

5.1 Introduction

The graphics boards are mostly an assemblage of "black box" parts and there isn't a lot of external logic that goes between them. Thus, the following sections don't provide much programming information about the chips themselves. That is left to the published information. Section 1.3 provides a list of appropriate publications that include manufacturer's data sheets and manuals.

Rather, the following sections just summarize the devices and but mostly focus on "hints and kinks". They are intended to supply information unique to the use of the chip on the graphics board.

Rastergraf offers a variety of software to support these graphics boards running under Windows 2000 and XP, VxWorks, and Linux. These offerings are covered in detail on the Rastergraf web page (http://www.rastergraf.com/).

Note

Please read these sections **before** starting on this chapter:

Section 1.2 Functional description.
Chapter 4 Installation

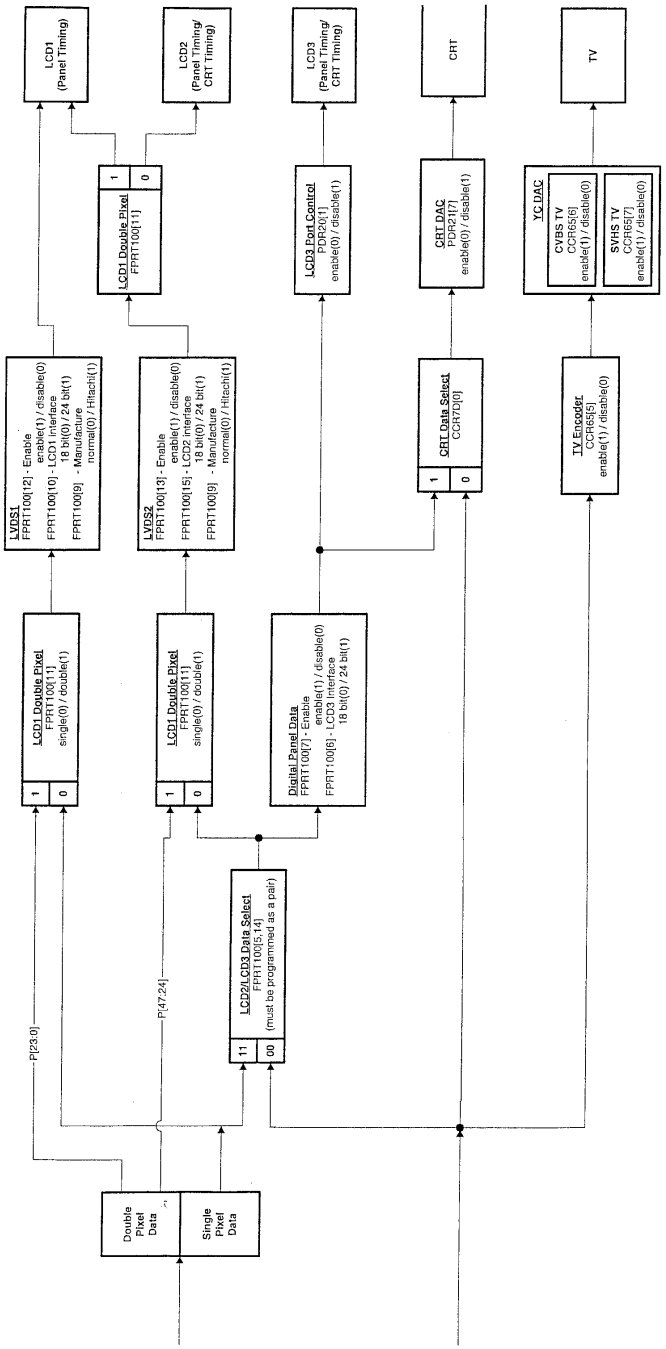
This chapter includes the following other sections:

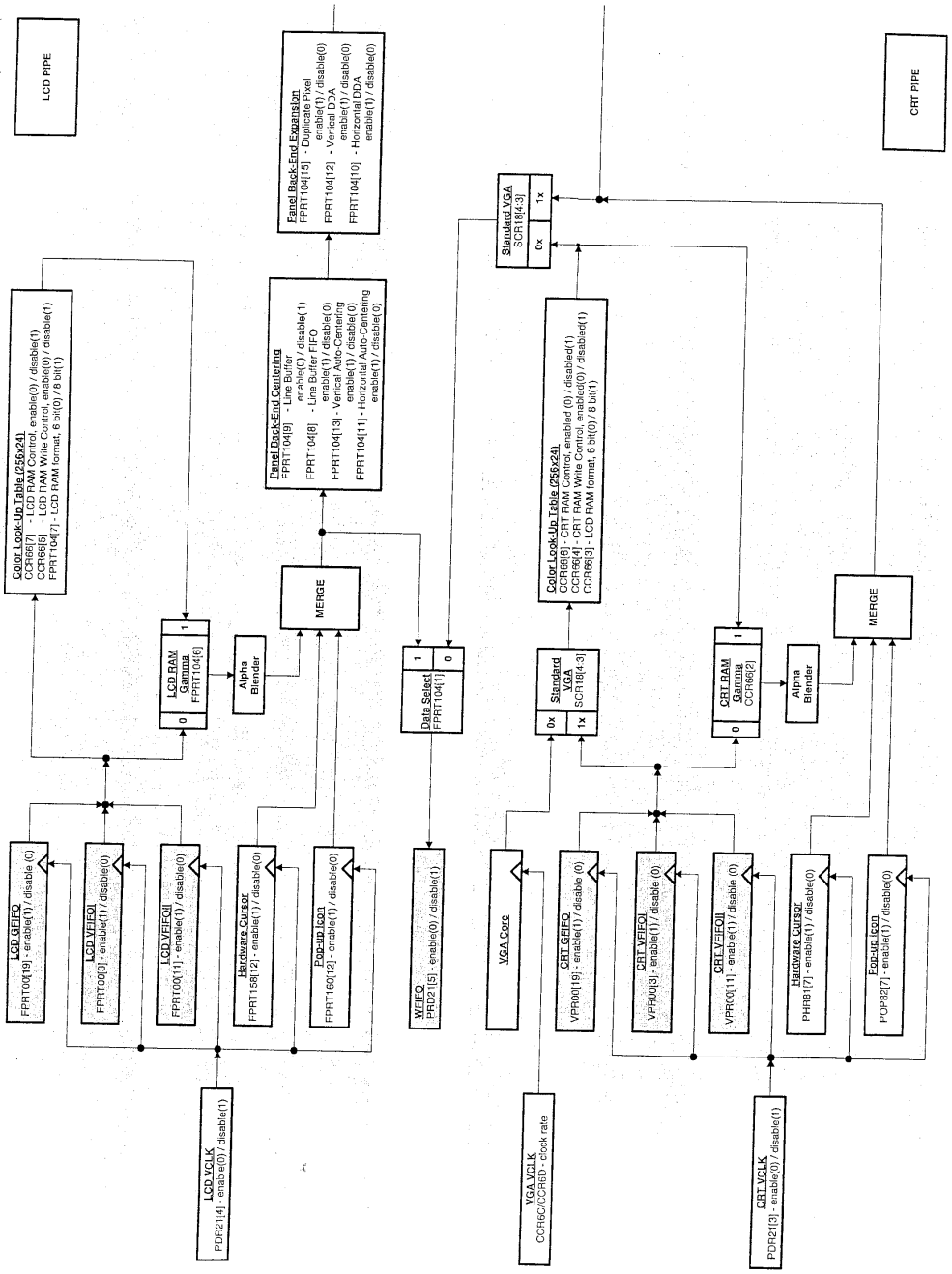
.

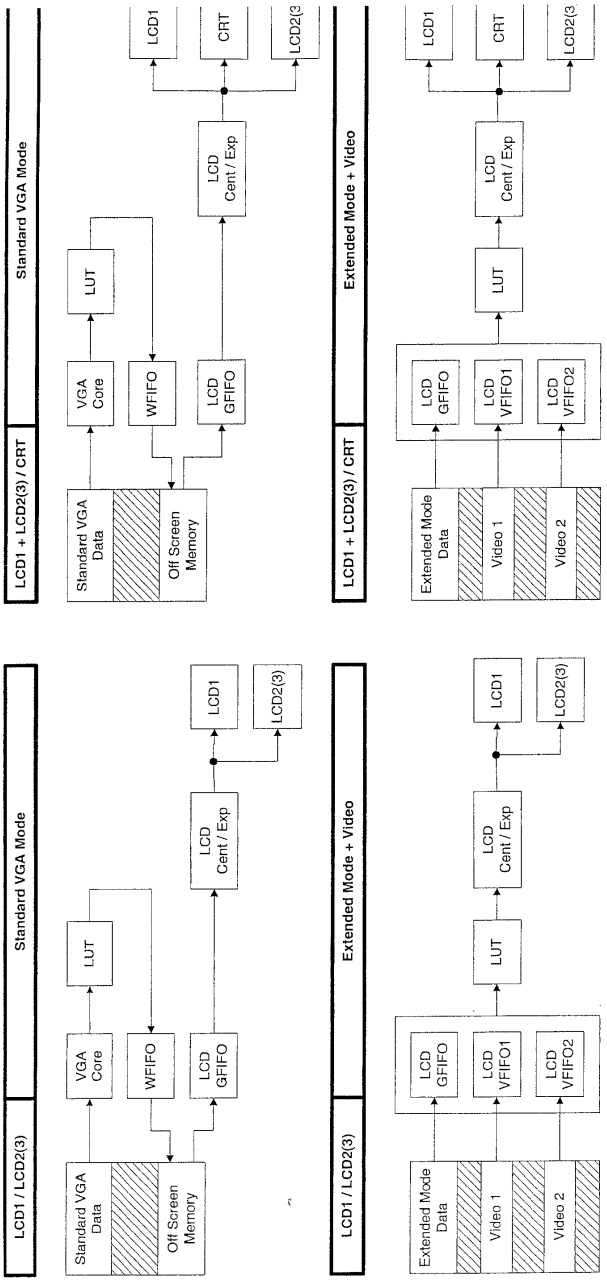
5.2 SM731 Graphics Accelerator

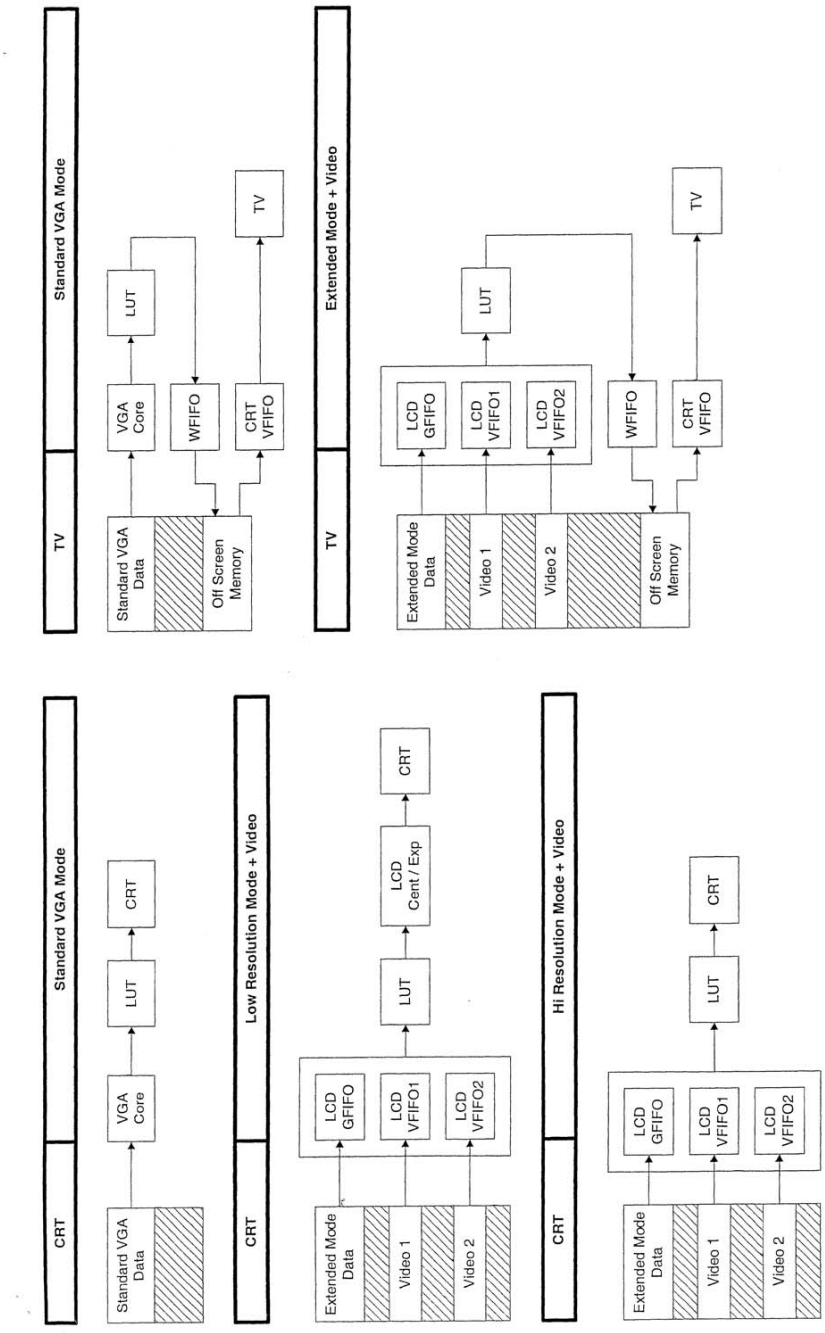
> **Note**
>
> The ***SM731 Technical Manual*** is available from Rastergraf under NDA.

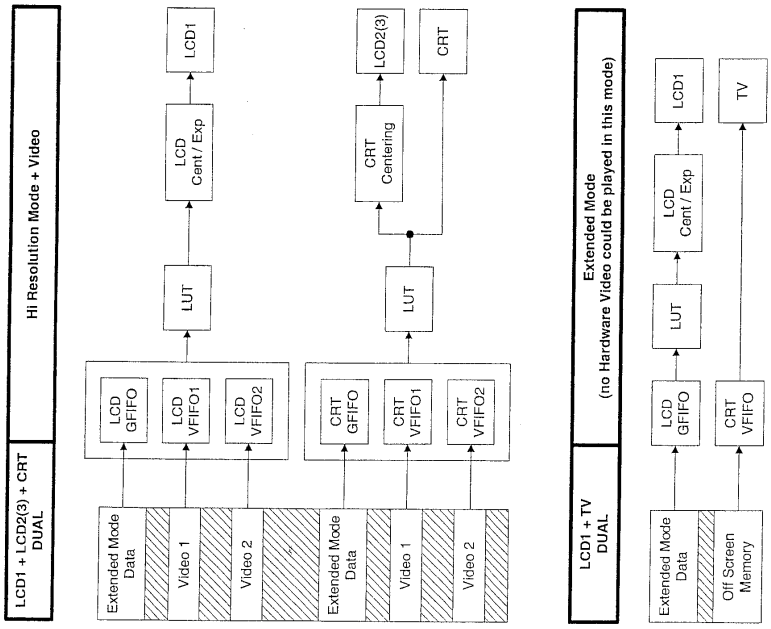
The following pages are scans and are a little blurry, but they contain a wealth of information not obtainable elsewhere that shows how the SM731 clocks and display functions are implemented.

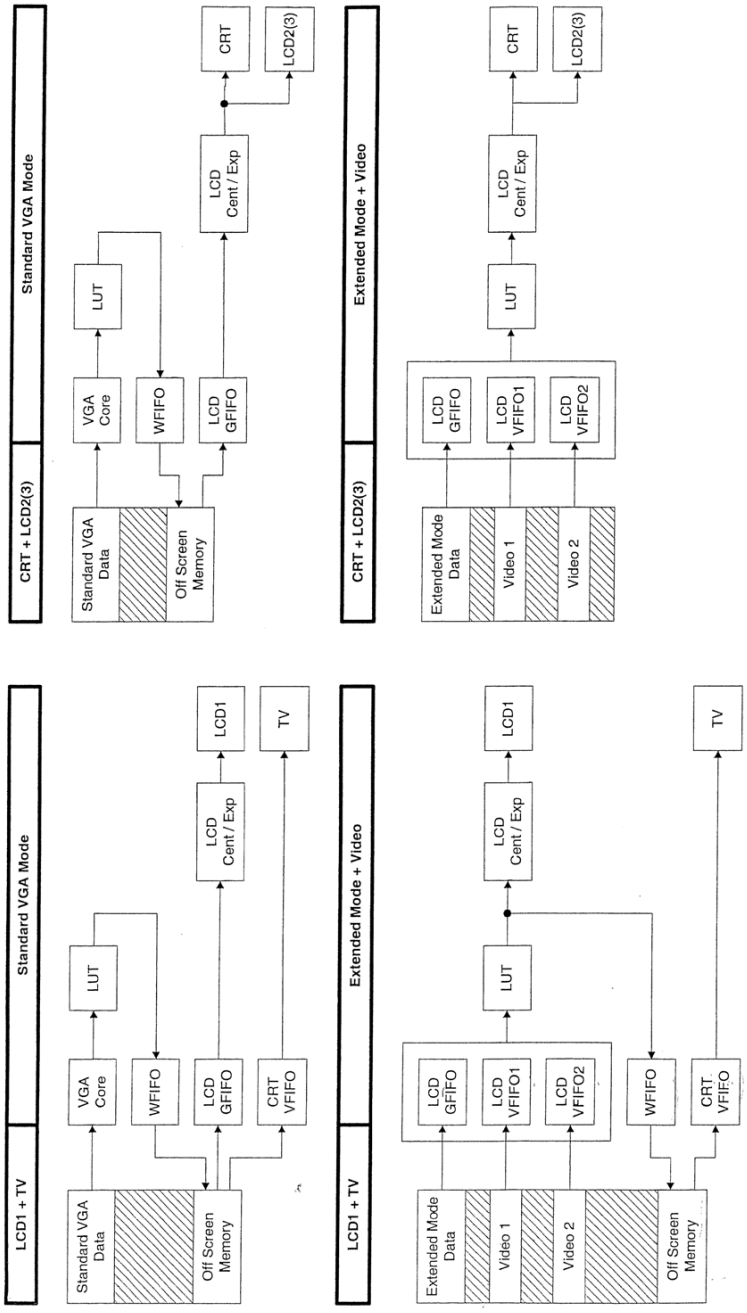

LCD1 (Panel Timing)
LCD2 (Panel Timing/ CRT Timing)
LCD3 (Panel Timing/ CRT Timing)
CRT
TV
LCD1 Double Pixel FPRT100[11]
1
0
LVDS1 FPRT100[12] - Enable enable(1) / disable(0) FPRT100[10] - LCD1 interface 18 bit(0) / 24 bit(1) FPRT100[9] - Manufacture normal(0) / Hitachi(1)
LVDS2 FPRT100[13] - Enable enable(1) / disable(0) FPRT100[15] - LCD2 interface 18 bit(0) / 24 bit(1) FPRT100[9] - Manufacture normal(0) / Hitachi(1)
LCD3 Port Control PDR20[1] enable(0) / disable(1)
CRT DAC PDR21[7] enable(0) / disable(1)
YC DAC
CVBS TV CCR65[6] enable(1) / disable(0)
SVHS TV CCR65[7] enable(1) / disable(0)
CRT Data Select CCR70[0]
TV Encoder CCR65[5] enable(1) / disable(0)
Digital Panel Data FPRT100[7] - Enable enable(1) / disable(0) FPRT100[6] - LCD3 interface 18 bit(0) / 24 bit(1)
LCD2/LCD3 Data Select FPRT100[5,4] (must be programmed as a pair)
11
00
P[23:0]
P[47:24]
Double Pixel Data
Single Pixel Data

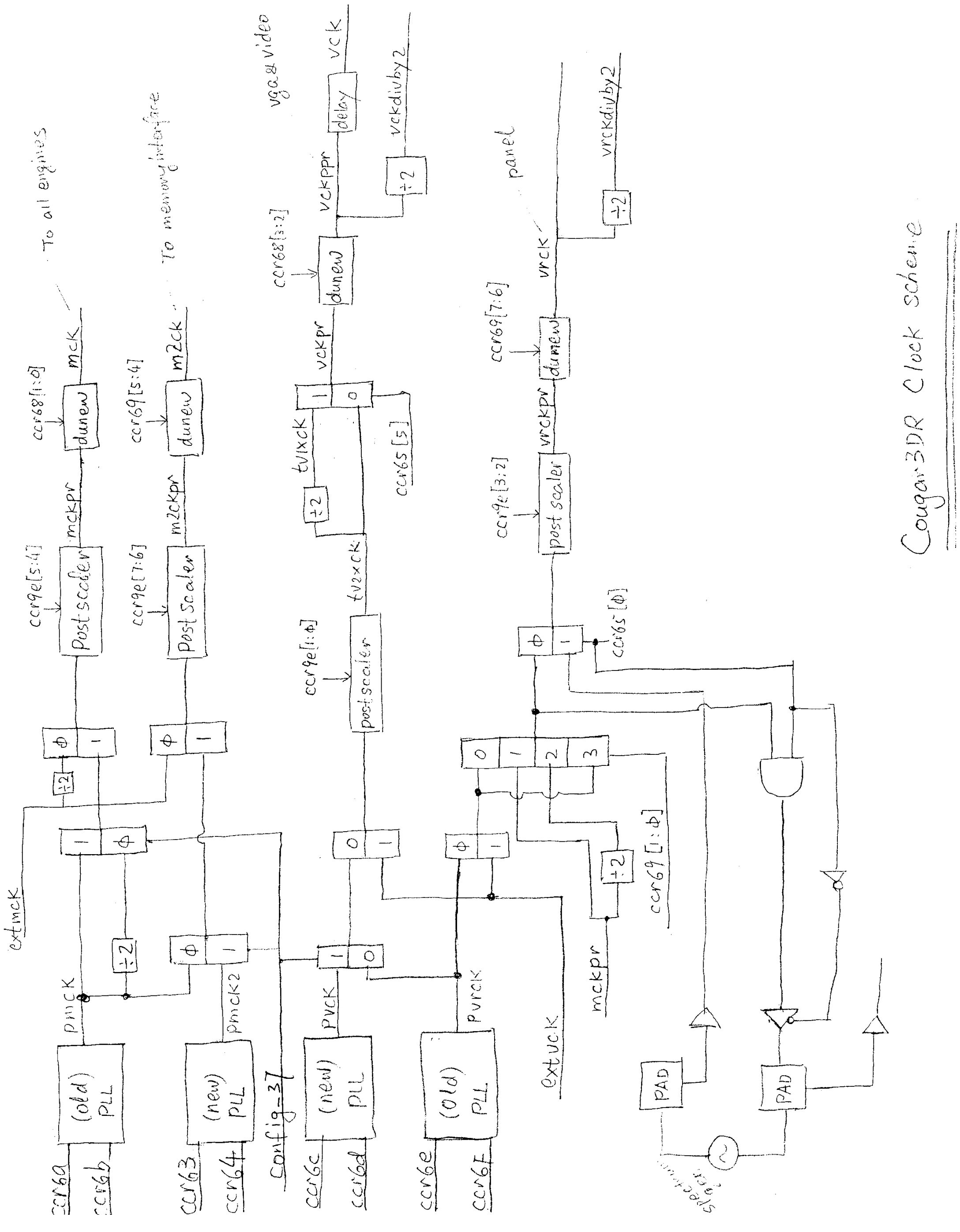

LCD PIPE
CRT PIPE
Color Look-Up Table (256x24)
CCR66[7] - LCD RAM Control, enable(0) / disable(1)
CCR66[6] - LCD RAM Write Control, enable(0) / disable(1)
FPRT104[7] - LCD RAM format, 6 bit(0) / 8 bit(1)
LCD RAM Gamma
FPRT104[6]
Alpha Blender
MERGE
Panel Back-End Centering
FPRT104[9] - Line Buffer
enable(0) / disable(1)
FPRT104[8] - Line Buffer FIFO
enable(1) / disable(0)
FPRT104[13] - Vertical Auto-Centering
enable(1) / disable(0)
FPRT104[11] - Horizontal Auto-Centering
enable(1) / disable(0)
Panel Back-End Expansion
FPRT104[15] - Duplicate Pixel
enable(1) / disable(0)
FPRT104[12] - Vertical DDA
enable(1) / disable(0)
FPRT104[10] - Horizontal DDA
enable(1) / disable(0)
Data Select
FPRT104[1]
LCD GFIFO
FPRT100[19] - enable(1) / disable (0)
LCD VFIFO1
FPRT100[3] - enable(1) / disable(0)
LCD VFIFO2
FPRT100[11] - enable(1) / disable(0)
Hardware Cursor
FPRT158[12] - enable(1) / disable(0)
Pop-up Icon
FPRT160[12] - enable(1) / disable(0)
LCD VCLK
PDR21[4] - enable(0) / disable(1)
WFIFO
PRD2[5] - enable(0) / disable(1)
Standard VGA
SCR18[4:3]
Color Look-Up Table (256x24)
CCR66[5] - CRT RAM Control, enabled (0) / disabled(1)
CCR66[4] - CRT RAM Write Control, enable(0) / disabled(1)
CCR66[3] - LCD RAM format, 6 bit(0) / 8 bit(1)
CRT RAM Gamma
CCR66[2]
VGA Core
CRT GFIFO
VPR00[19] - enable(1) / disable (0)
CRT VFIFO1
VPR00[3] - enable(1) / disable (0)
CRT VFIFO2
VPR00[11] - enable(1) / disable (0)
Hardware Cursor
PHR81[7] - enable(1) / disable(0)
Pop-up Icon
POP82[7] - enable(1) / disable(0)
VGA VCLK
CCR6C/CCR6D - clock rate
CRT VCLK
PDR21[3] - enable(0) / disable(1)

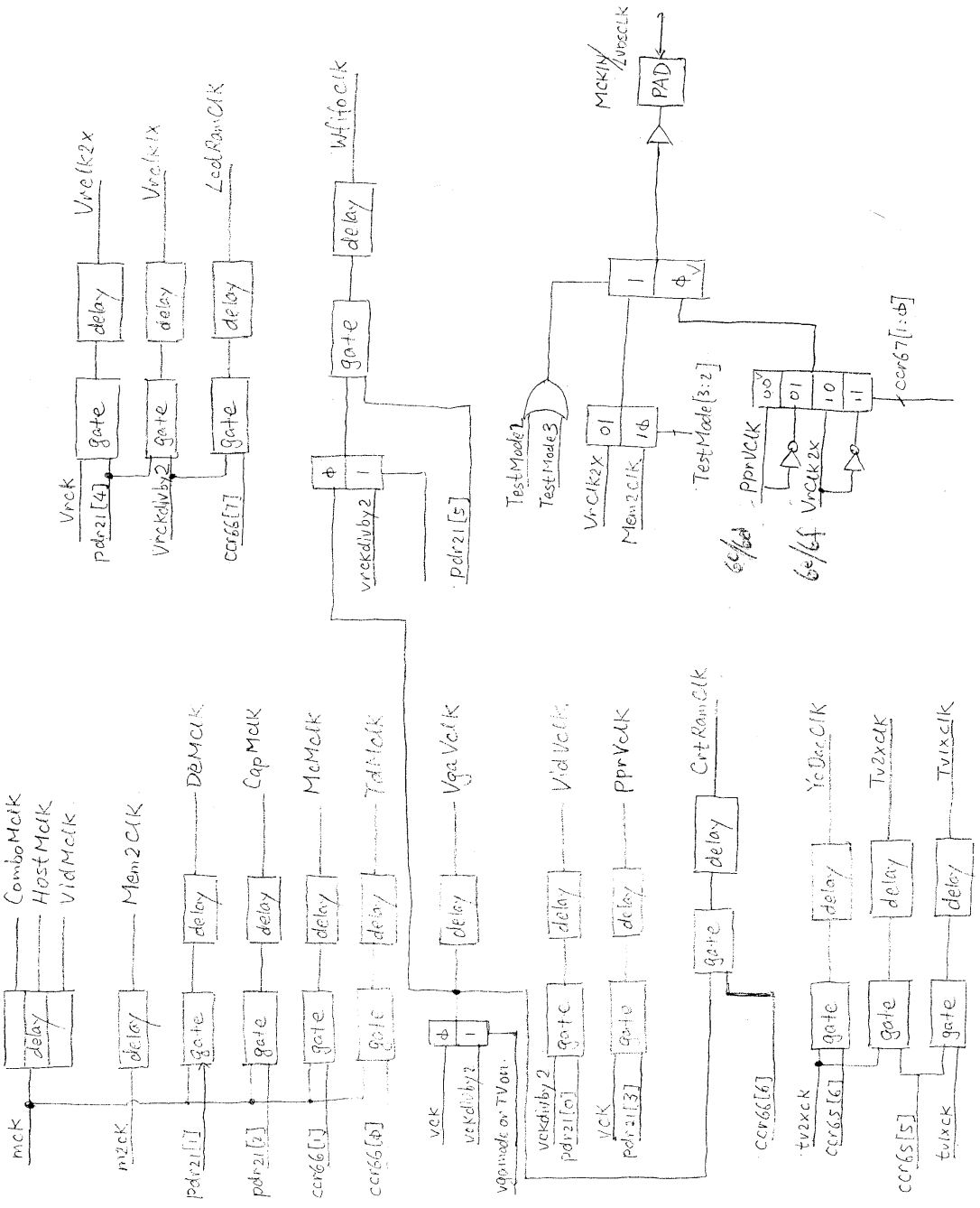

LCD1 + LCD2(3) / CRT
Standard VGA Mode
Standard VGA Data
Off Screen Memory
VGA Core
LUT
WFIFO
LCD GFIFO
LCD Cent / Exp
LCD1
CRT
LCD2(3
LCD1 + LCD2(3) / CRT
Extended Mode + Video
Extended Mode Data
Video 1
Video 2
LCD GFIFO
LCD VFIFO1
LCD VFIFO2
LUT
LCD Cent / Exp
LCD1
CRT
LCD2(3
LCD1 / LCD2(3)
Standard VGA Mode
Standard VGA Data
Off Screen Memory
VGA Core
LUT
WFIFO
LCD GFIFO
LCD Cent / Exp
LCD1
LCD2(3)
LCD1 / LCD2(3)
Extended Mode + Video
Extended Mode Data
Video 1
Video 2
LCD GFIFO
LCD VFIFO1
LCD VFIFO2
LUT
LCD Cent / Exp
LCD1
LCD2(3)


TV
Standard VGA Mode
Standard VGA Data
Off Screen Memory
VGA Core
LUT
WFIFO
CRT VFIFO
TV
TV
Extended Mode + Video
Extended Mode Data
Video 1
Video 2
Off Screen Memory
LCD GFIFO
LCD VFIFO1
LCD VFIFO2
LUT
WFIFO
CRT VFIFO
TV
CRT
Standard VGA Mode
Standard VGA Data
VGA Core
LUT
CRT
CRT
Low Resolution Mode + Video
Extended Mode Data
Video 1
Video 2
LCD GFIFO
LCD VFIFO1
LCD VFIFO2
LUT
LCD Cent / Exp
CRT
CRT
Hi Resolution Mode + Video
Extended Mode Data
Video 1
Video 2
LCD GFIFO
LCD VFIFO1
LCD VFIFO2
LUT
CRT


LCD1 + LCD2(3) + CRT DUAL
Hi Resolution Mode + Video
Extended Mode Data
Video 1
Video 2
LCD GFIFO
LCD VFIFO1
LCD VFIFO2
LUT
LCD Cent / Exp
LCD1
CRT GFIFO
CRT VFIFO1
CRT VFIFO2
LUT
CRT Centering
LCD2(3)
CRT
LCD1 + TV DUAL
Extended Mode
(no Hardware Video could be played in this mode)
Extended Mode Data
Off Screen Memory
LCD GFIFO
CRT VFIFO
LUT
LCD Cent / Exp
LCD1
TV


CRT + LCD2(3)
Standard VGA Mode
Standard VGA Data
Off Screen Memory
VGA Core
LUT
WFIFO
LCD GFIFO
LCD Cent / Exp
CRT
LCD2(3)
CRT + LCD2(3)
Extended Mode + Video
Extended Mode Data
Video 1
Video 2
LCD GFIFO
LCD VFIFO1
LCD VFIFO2
LUT
LCD Cent / Exp
CRT
LCD2(3)
LCD1 + TV
Standard VGA Mode
Standard VGA Data
Off Screen Memory
VGA Core
LUT
WFIFO
LCD GFIFO
CRT VFIFO
LCD Cent / Exp
LCD1
TV
LCD1 + TV
Extended Mode + Video
Extended Mode Data
Video 1
Video 2
Off Screen Memory
LCD GFIFO
LCD VFIFO1
LCD VFIFO2
LUT
WFIFO
CRT VFIFO
LCD Cent / Exp
LCD1
TV


Cougar3DR Clock scheme
To all engines
To memory interface
vga & video
panel
mck
m2ck
vck
vckdivby2
vrck
vrckdivby2
mckpr
m2ckpr
vckpr
vckppr
vrckpr
delay
dunew
Post scaler
extmck
extvck
pmck
pmck2
pvck
pvrck
(old) PLL
(new) PLL
PAD
ccr6a
ccr6b
ccr63
ccr64
ccr6c
ccr6d
ccr6e
ccr6F
config-37
tv1xck
tv2xck
ccr65[5]
ccr65[0]
ccr68[1:0]
ccr68[3:2]
ccr69[5:4]
ccr69[7:6]
ccr69[1:0]
ccr9e[5:4]
ccr9e[7:6]
ccr9e[1:0]
ccr9e[3:2]


mclk
ComboMclk
HostMclk
VidMclk
delay
m2clk
Mem2Clk
pdr21[1]
gate
DeMclk
pdr21[2]
CapMclk
ccr66[1]
McMclk
ccr66[0]
TdMclk
vclk
vclkdiby2
vgamode or TVon
VgaVclk
vclkdiby2
pdr21[0]
VidVclk
VCK
pdr21[3]
PprVclk
ccr66[6]
CrtRamClk
tv2xck
ccr65[6]
YcDacClk
ccr65[5]
Tv2xclk
tv1xclk
Tv1xclk
Vrck
pdr21[4]
Vrclk2x
Vrclk1x
vrckdiby2
LcdRamClk
ccr66[7]
WfifoClk
pdr21[5]
TestMode2
TestMode3
VrClk2x
01
10
Mem2Clk
TestMode[3:2]
MCKIN/2VDSCLK
PAD
PprVClk
00
01
10
11
VrClk2x
ccr67[1:0]

5.3 Clocks

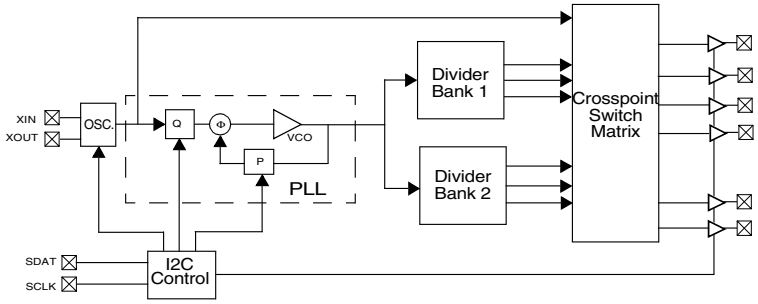
5.3.1 CY22150 Reference Clock

Because the SM731 video output encoder is sensitive to clock frequency, the Topaz, Duros, and Garnet have an enhanced clock circuit that permits the clock to be fine-tuned for optimum encoder operation.

A low-noise clock, the Cypress CY22150, programmed via an I^2C port, provides a highly stable clock.

Rastergraf software knows to look for the CY22150 and will program it accordingly.

Figure 5-1 CY22150 Block Diagram



5.4 Video Timing Parameters

The SM731 must be programmed to generate the proper video timing for the hardware configuration and display format. Rastergraf' SDL Graphics Package accepts display format (e.g., 1600 x 1200, 32 bpp) and refresh requirements (e.g., 67 Hz vertical refresh) as parameters to a function call. The software then provides (and loads) a best-fit timing profile for the SM731 graphics chip.

Does your Display have a Green Cast to it?

By default, the graphics board supplies video in separate (five wire video RGBHV) video format. If you hook the board up to a multiscan monitor with a regular VGA cable then you will be giving RGBHV to the monitor. Be sure to not select sync-on-green or you will get a green cast to the image.

Table 5-1 Standard Graphics Display Formats

Format Name	Pixel Resolution	Aspect Ratio
QXGA	2048 x 1536	4:3
WUXGA	1920 x 1200	8:5 (HDTV)
UXGA	1600 x 1200	4:3
SXGA+	1400 x 1050	4:3
SXGA	1280 x 1024	5:4
QVGA	1280 x 960	4:3
XGA	1024 x 768	4:3
SVGA	800 x 600	4:3
VGA	640 x 480	4:3

5.4.1 Application Note: Adjusting the Timing Parameters

Most monitors have adjustments for Horizontal Frequency, Horizontal Position, Horizontal Size, Vertical Frequency, Vertical Position and Vertical Size. It is recommended that the monitor adjustments be tried before trying monitor settings not in accord with the monitor data sheet.

Rastergraf' SDL software allows you to define the timing parameters in one of two ways:

a) you tell SDL that you are using a multiscan monitor. You specify the display active width and height (e.g., 1600 x 1200) and the Vertical Frequency, and the program figures out the rest.

b) you tell SDL exactly what you want the timing to be. You specify:

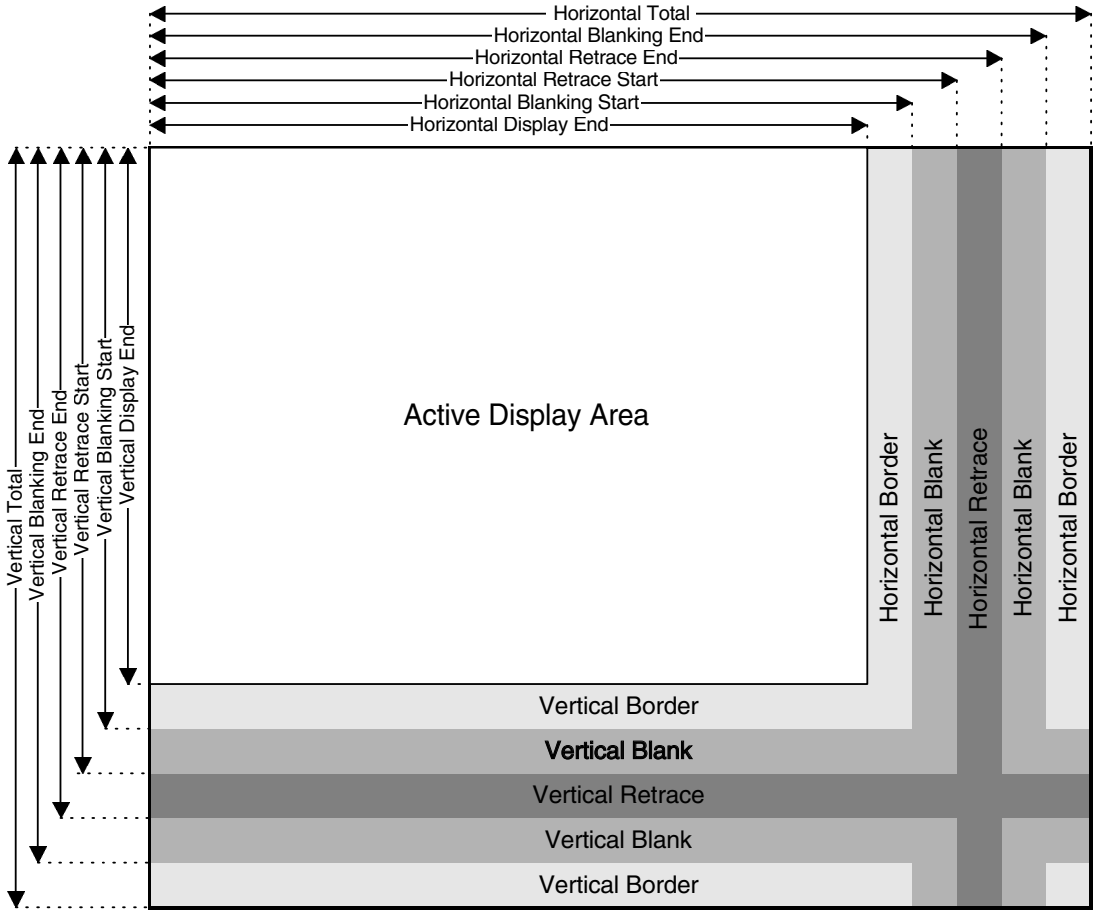
- vertical frequency in Hz
- vertical blanking in milliseconds (ms)
- vertical front porch in ms
- vertical sync width in ms
- horizontal blanking in microseconds (us)
- horizontal front porch in us
- horizontal sync width in us
- display width and height
-

The program derives the horizontal frequency from this information. Ordinarily, you should be able to use the monitor's data sheet to obtain a satisfactory display. However, it may be that adjustments are required. This section gives you some advice on how to do this. You can also send Rastergraf a filled-in copy of the parameters sheet which follows this section.

Declaration

Rastergraf is dedicated to making your application work. We can assist in determining special video timing parameters for specific monitors and other output devices. If you need help it would be very useful if you can gather the data requested in the following form before calling us.

Figure 5-2 Video Display Timing Fields



To change the horizontal frequency:

The horizontal frequency is also known as horizontal refresh rate or horizontal scan rate. Indications that the horizontal frequency needs to be changed are an unviewable picture with diagonal lines. Some monitors display no picture when the horizontal frequency is out of its bandwidth. The same symptoms can be caused by no sync at all, so make sure that the cables are connected correctly and that the monitor is configured correctly. When the picture is out of sync, the number of diagonal lines is an indication of how close to the correct horizontal frequency you are: fewer lines are closer, more lines are farther. Remember that changing the horizontal frequency will also affect the vertical frequency. Decreasing the horizontal frequency will generally result in a wider picture.

To change the horizontal position:

To shift the image *left* **increase** the horizontal front porch by the same amount. Perform the converse procedure to move the image to the *right*.

To change the width of the image:

The best way to change the width of the image is to change the pixel clock frequency. If you want to change the pixel clock but not any other timing parameters, then increasing the frequency will result in a narrower image and decreasing it will result in a wider image While there are ways to change the width (horizontal size) of the image without changing the pixel clock, they affect other timing parameters and can lead to complications.

> **Note:**
>
> To keep the timing intervals the same when changing the pixel clock you have to enter new horizontal timing parameters.

To change the vertical frequency:

The vertical frequency is also known as vertical refresh rate or vertical scan rate. Indications that the vertical frequency needs to be changed are a picture which rolls up or down. Sometimes the appearance is of multiple pictures, one on top of another, with multiple horizontal lines. A very slow vertical frequency will cause the image to flicker. Some monitors display no picture when the vertical frequency is out of its bandwidth. Since the same symptoms can be caused by no sync at all, make sure that the cable is connected correctly and that the monitor is configured correctly.

To change the vertical position:

To shift the image *up* **increase** the vertical front porch by the same amount. Perform the converse procedure to move the image *downward*.

To change the height of the image:

There are two ways to change the height (vertical size) of the image.

1) Change the number of lines. The image aspect ratio remains the same.
2) Change the vertical frequency. Increasing the vertical frequency will result in a shorter image, decreasing it will result in a taller image.

5.4.2 Pan and Scroll

Panning and scrolling (also called roaming) are techniques used to provide a window into a larger memory than can be displayed. The display X (pan) and Y (scroll) starting points are changed, allowing new data areas to be displayed. This function is appropriate when using a display format which doesn't use up all of memory. For example, a 16 MB board with a 1280 x 1024 x 8 bpp format gives you ***almost thirteen*** full screens to roam around in. Routines in the Rastergraf SDL software provide you with an easy way to pan and scroll in memory.

Table 5-2 Video Timing Parameter Request Form

Request for Assistance in Determining Video Timing Parameters

Submit to: Rastergraf, Inc.
1810-J SE First St.
Redmond, OR 97756
(541) 923-5530
email: support@rastergraf.com

Company Information
Company Name_____
Contact_____
Phone Number_____
email_____

Monitor Information
Monitor Brand_____ Model Number_____

Graphics Board Information
Model Number_____ Serial Number_____

Horizontal Timing Information
Note: Horizontal timings may be given in pixel units (if given) or time units.
Horizontal Pixels per Line Displayed_____
Pixel Time or Frequency (optional)_____
Horizontal Total Line Time or Frequency_____
Horizontal Front Porch_____
Horizontal Sync Width_____
Horizontal Back Porch_____

Vertical Timing Information
Note: Vertical timings may be given in line units or time units.
Vertical Lines Displayed_____
Vertical Lines Total or Frequency (Field Rate)_____
Vertical Front Porch_____
Vertical Sync Width_____
Vertical Back Porch_____

Sync Information
Sync Polarity (+ or -): Composite:_____ Horizontal:_____ Vertical:_____

Additional Notes
_____
_____

5.5 System Management Devices and Functions

The Topaz/Stratus/Garnet boards have devices that are specifically intended to assist in system management. These include:

- A National Semiconductor LM75 I^2C temperature sensor located near the SM731 chip provides local temperature measurements. You can obtain the data sheet and collateral information for the LM75 from the technical document section on the Rastergraf web site;
- A 2 Kb I^2C Serial EEPROM which can be used by system software to store data such as serial number and software revision;
- In addition, there are features of the SM731 chip that are useful:
- Power management control registers allow various parts of the chip to be put powered down without making the chip entirely useless;
- Signature registers in the RAMDAC can be are used to confirm that a test pattern in display memory will pass correctly through the SM731 all the way to the DAC inputs. This is useful as a Built In Self Test (BIST) function;
- When the board is properly connected to a monitor and a test image is displayed on the monitor, a certain level voltage will be developed at the DAC outputs that drive the monitor. A simple A/D reads the voltage and confirms that the DAC output is above a certain threshold level;
- The I^2C-based DDC2B protocol is used to control the display monitor. DDC2B is a VESA standard (http://www.vesa.org/) which allows the frame buffer to read the Additional Display Identification Data (EDID) from the monitor. The EDID includes resolutions supported, maximum width and refresh, and sync type;
- Frequency select bits for the SM731 Drawing Engine and the programmable Memory Clock PLL allow the system to optimize operating frequencies for the SM731 as a function of system temperature.

Please contact Rastergraf for more information if you wish to utilize any or all of these features.

5.6 Talk To Me Through I^2C

The SM731 chip has a control register that is used to implement the I^2C protocol, a 2 wire serial bus designed by Philips Semiconductor. The SM731 is the I^2C master and it controls the bus through the DDC control register in the SM731 chip. The I^2C bus supports specific "start", "stop" and "acknowledge" states, so it is possible to probe for these devices and determine whether they exist.

I^2C is used to control the following devices:

CY22150 clock (Topaz, Garnet, Duros)
THC63DV164 DVI digital video encoder/transmitter,
LM75 thermal sensor,
AT24C02 2 Kbit serial EEPROM, and
the Display Monitor,

An I^2C device is determined by a combination of device internal bits (bits 4-7) and (usually) three pins that are wired by the board designer (bits 1-3) Bit 0 is used to denote a Read (1) or Write (0) operation.

The LM75 must be read in 2 byte increments, otherwise it will hang the I^2C bus. Since most vendors combine the R/W bit with the actual I^2C address (e.g., write @ 0x88, read @ 0x89), the following table uses that convention.

Table 5-3 I^2C Device Addresses

Device	R/W	Hex	I2C Bus
CY22150 Reference Clock	W	0x68	1
	R	0x69	1
THC63DV164	W	0x70	1
	R	0x71	1
LM75	W	0x9C	1
	R	0x9D	1
AT24C02	W	0xA8	1
	R	0xA9	1
Display Monitor	W	0xA8	0
	R	0xA9	0

5.7 Topaz/Stratus/Garnet Auxiliary Register

The Topaz/Stratus/Garnet versions have an auxiliary register that is accessed through the SM731 secondary I^2C bus (USR2/3) and is located in a Lattice M4A3-64/64, IC U30. The register controls the sync mode and the data path between the Bt835 and AD9882 digitizer chips and SM731.

I^2C addresses on secondary I^2C bus (USR2/3)

"0x60 PCSR (Rastergraf Control Status Register) write\n"
"0x61 PCSR (Rastergraf Control Status Register) read\n"

Bit	Mnemonic	Description
0	BTPwrOff	Set to enable AD9882 to drive the SM731 VIP
1	Datamode	Set for AD9882 monochrome when receiving analog YUV input. Luminance is set to 0x80.
2	VideoLoopback	Set to loop SM731 VOUT to Bt835 VIN1
3	SOGoutPri	Set to enable SOG on primary DAC
4	SOGoutSec	Set to enable SOG on secondary DAC
5	SecDAC	Set to enable the secondary DAC
6	BlockSOGPri	0 for XOR SOG, 1 for block SOG
7	BlockSOGSec	0 for XOR SOG, 1 for block SOG

BlockSOGPri	SOGoutPri	Description
0	0	No SOG on primary DAC
0	1	XOR SOG on primary DAC
1	0	Reserved for special modes – do not use
1	1	Block SOG on primary DAC

5.8 DVI Digital Video Output

General Description

The THC63DV164 transmitter uses DVI Digital technology to support displays ranging from VGA to UXGA resolutions (25-165Mpix/s) in a single link interface. As used on these Rastergraf boards, the THC63DV164 transmitter is connected to the SM731 via a 24-bit mode, one pixel per clock edge interface. The THC63DV164 is programmed though an I^2C slave interface, eliminating the requirement for external programming pins. The THC63DV164 supports Receiver Detection for a variety of power management options.

Features

- 25 - 165 Megapixels/sec (VGA to UXGA)
- Uses 24-bit single clock, dual edge (24-bit pixel data)
- I^2C Slave Programming Interface
- Receiver Detection: Supports Hot Plug Detection
- De-skewing option: varies clock to data timing
- Supports cable length over 5m with twisted pair, fiber-optics ready
- DVI 1.0 compatible

Data Sheet

You can obtain the data sheet and collateral information for the THC63DV164 from the technical document section on the Rastergraf web site.

Figure 5-3 THC63DV164 Block Diagram

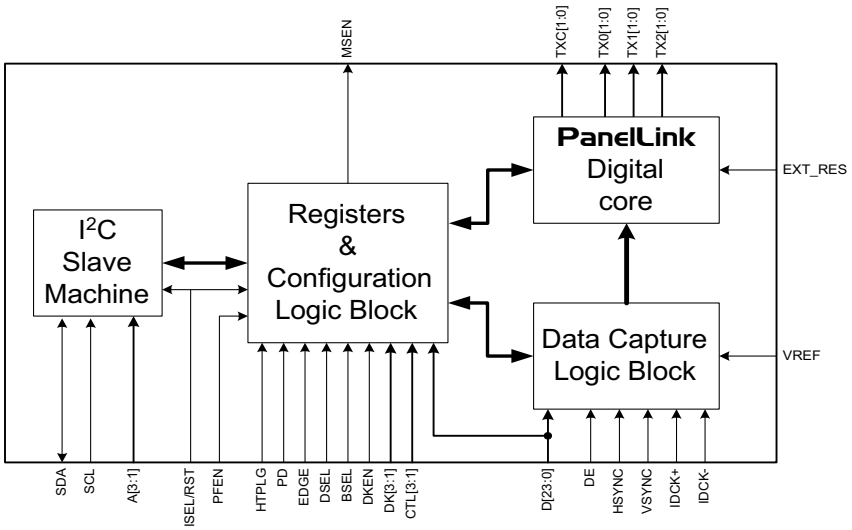
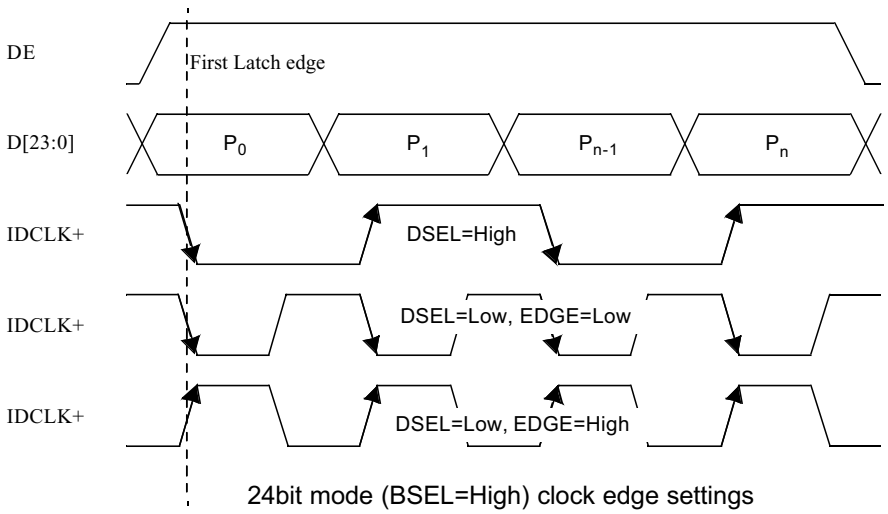


Figure 5-4 THC63DV164 RGB to 24-bit TMDS Mapping Diagram



Notes: In 24 bit Single Clock Dual Edge mode, the THC63DV164 will look at the first clock edge (either falling or rising) after DE goes high to determine the first pixel data. EDGE pin has no affect in 24 bit Single Clock Dual Edge mode.

24bit Mode Data Mapping Table

	P0	P1		Pn
D23	R0[7]	R1[7]		Rn[7]
D22	R0[6]	R1[6]		Rn[6]
D21	R0[5]	R1[5]		Rn[5]
D20	R0[4]	R1[4]		Rn[4]
D19	R0[3]	R1[3]		Rn[3]
D18	R0[2]	R1[2]		Rn[2]
D17	R0[1]	R1[1]		Rn[1]
D16	R0[0]	R1[0]		Rn[0]
D15	G0[7]	G1[7]		Gn[7]
D14	G0[6]	G1[6]		Gn[6]
D13	G0[5]	G1[5]		Gn[5]
D12	G0[4]	G1[4]		Gn[4]
D11	G0[3]	G1[3]		Gn[3]
D10	G0[2]	G1[2]		Gn[2]
D9	G0[1]	G1[1]		Gn[1]
D8	G0[0]	G1[0]		Gn[0]
D7	B0[7]	B1[7]		Bn[7]
D6	B0[6]	B1[6]		Bn[6]
D5	B0[5]	B1[5]		Bn[5]
D4	B0[4]	B1[4]		Bn[4]
D3	B0[3]	B1[3]		Bn[3]
D2	B0[2]	B1[2]		Bn[2]
D1	B0[1]	B1[1]		Bn[1]
D0	B0[0]	B1[0]		Bn[0]

Notes: [1]In this figure, clock edges represented by arrows signify latching edge.
[2]Color pixel components are represented as R:Red, G:Green and B:Blue.
[3]Bit significance with in a color: [7:0] = [MSB:LSB]

5.9 ADV7123 and ADV7120 VGA DACs

The Stratus uses the ADV7123 and the Duros/Garnet use the ADV7120. Both are triple high speed, digital-to-analog converter on a single monolithic chip. It consists of three high-speed, 10-bit, video D/A converters with complementary outputs, a standard TTL input interface and a high impedance, analog output current source.

The ADV7120 has additional inputs for black level and full white which are required to support the STANAG A option.

For more information, see the ADV7120 Data Sheet:

http://www.analog.com/UploadedFiles/Data_Sheets/173587347adv7120.pdf

or,

For more information, see the ADV7123 Data Sheet:

http://www.analog.com/UploadedFiles/Data_Sheets/276580127ADV7123_b.pdf

5.10 AD9882 High Speed Digitizer (Stratus/Garnet)

Analog Interface

The AD9882 is a complete 8-bit 140 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full power analog bandwidth of 300 MHz supports resolutions up to SXGA (1280 x 1024 at 75 Hz). The analog interface includes a 140 MHz triple ADC with internal 1.25 V reference, a Phase Locked Loop (PLL), and programmable gain, offset, and clamp control. The AD9882's on-chip PLL generates a pixel clock from Hsync. Pixel clock output frequencies range from 12 MHz to 140 MHz. PLL clock jitter is typically 500 ps p-p at 140 MSPS. The AD9882 also offers full sync processing for composite sync and Sync-on-Green (SOG) applications.

Digital Interface

The AD9882 contains a DVI 1.0 compatible receiver and supports display resolutions up to SXGA (1280 ¥ 1024 at 60 Hz). The receiver features an intra-pair skew tolerance of up to one full clock cycle.

For more information, see the AD9882 Data Sheet:

http://www.analog.com/UploadedFiles/Datasheets/415000914AD9882_a.pdf

5.11 Bt835 NTSC/PAL/SECAM Video Decoder

Note: this section is derived from Conexant's Bt835 Product Brief

What is a Video Decoder?

A video decoder is a chip that allows live video from a television broadcast, a video tape or a camera to be brought into a computer. To accomplish this, the chip must first track the video signal, digitize it, separate out the brightness and color information from the signal, and send the digital ones and zeros representing the video signal to the computer's video subsystem. Once captured, the digital bits representing the video image can be manipulated by video-related applications.

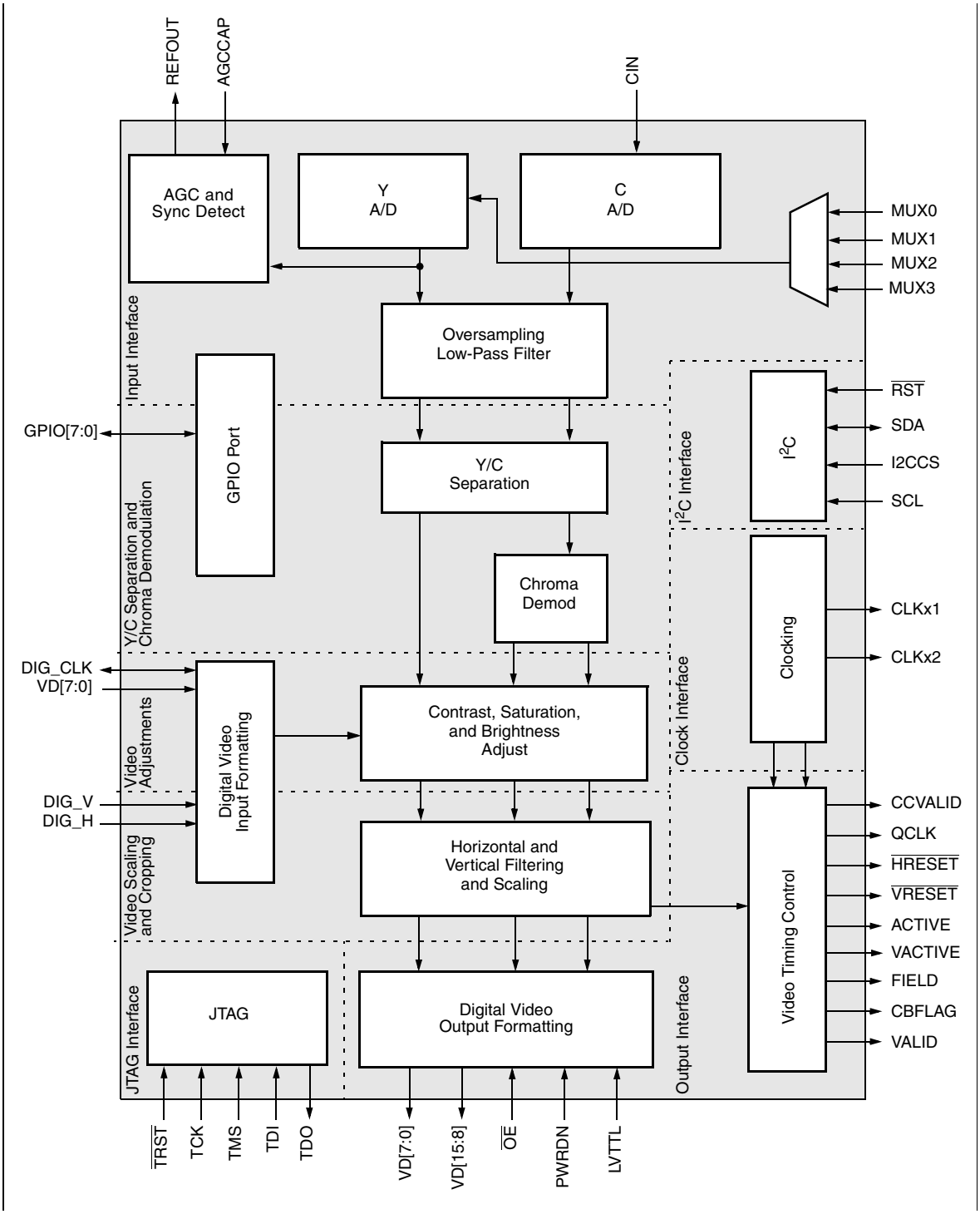
Features

- Digitizes composite, S-video, and NTSC/PAL/SECAM to YCrCb
- Square pixel and CCIR601 resolution for NTSC, PAL, and SECAM
- 2H adaptive comb filtering (NTSC)
- High quality horizontal and vertical filtered down-scaling
- Closed caption and VBI data decoding
- Vertical blanking interval data pass-through
- Programmable temporal decimation for a reduced frame-rate video
- Programmable hue, brightness, saturation, and contrast
- Two-wire I^2C bus interface
- Software selectable four-input analog multiplexer
- Auto NTSC/PAL format detect and gain control
- User programmable peaking filter

- Introduction

The Conexant Bt835 video capture processor is a single-chip decoding and filtered scaling solution for analog NTSC/PAL/SECAM base-band signals from TV tuners, VCRs, cameras, and other sources of composite or Y/C video. The Bt835 is a video-capture solution that integrates video digitization, synchronization, 2H adaptive Y/C separation, scaling and VBI data pass-through functions. Using mixed signal and DSP circuitry, the Bt835 converts an analog composite video waveform into a scaled digital video stream while supporting a variety of video formats.

Figure 5-5 Bt835 Detailed Block Diagram



Analog Video Input Interface

The Bt835 supports composite and S-video sources in NTSC, PAL, and SECAM video formats. Four composite, or three composite and one S-video sources are selected through an on-chip 4:1 analog multiplexer. The Bt835 integrates two flash Analog-to-Digital Converters (ADCs) which provide high-performance 8x oversampling of the NTSC/PAL color subcarrier. Oversampling of the analog signal enables simple external anti-aliasing filters and enhances digital filtering performance on-chip.

An on-chip PLL multiplies a 14.318 MHz reference frequency to 28.64 MHz for NTSC and 35.48 MHz for PAL, for 8x Fsc sampling of the baseband video signal. The fixed, integral relationship between the subcarrier frequency (Fsc) and the sample rate optimizes the performance of the Y/C separation. The Bt835 also incorporates auto-format detect capability through which it can sense the presence of an NTSC, PAL, or SECAM video source on the input after power up and configure itself accordingly.

Ultralock™

Employing Conexant patented Ultralock technique, the Bt835 achieves both horizontal and subcarrier synchronization to the incoming analog video signal. It will always generate the required number of pixels per line from an analog source in which the line length can vary by as much as a few microseconds. Ultralock‘s digital locking circuitry enables the Bt835 to quickly and accurately lock on to virtually any video signal. Since the technique is completely digital, Ultralock can recognize unstable signals caused by VCR headswitches or any other deviation and adapt the locking mechanism to accommodate the source. Ultralock uses non-linear techniques that adapt the locking mechanism automatically. This removes the requirement a conventional genlock circuit to reset the locking range to accommodate a particular system setup.

Digital Video Output Interface

The video pixels are delivered as a continuous video stream running at a 4x Fsc rate which is synchronous to the ADC sample clock. YCrCb and YUV 4:2:2 pixels are provided over an 8-bit data bus to the SM731, using data and clock which operate at 2x the video pixel rate. The Bt835 also has the capability of embedding the video control signals in the digital pixel stream in either ViP mode or ByteStream mode. The video field/frame synchronization signals and others are coded into the pixel data stream using out-of-range luminance and chrominance data values.

Vertical Blanking Interval Data Capture

The Bt835 captures and decodes Vertical Blanking Interval (VBI) data by operating in VBI line output mode, in which the VBI data is only captured during select lines. This mode of operation enables the concurrent capturing of VBI lines which contain ancillary data and the processing of normal video image data. In addition, the Bt835 supports a VBI frame output mode in which every line in the video frame is treated as if it were VBI line data. This mode is intended for still frame capture applications.

Scaling

The Bt835 provides a scaler for image ***downsizing***. The scale factor is arbitrary and independent in X and Y dimensions with a minimum scaling factor of 0.071. This enables full-resolution video to be reduced to any size down to icon resolution. The video can be optionally band-limited using a digital low-pass filter prior to scaling to minimize aliasing artifacts induced by the scaling process. Horizontal scaling is implemented through a six-tap 32-phase interpolation filter. Vertical scaling is performed with a multi-tap eight-phase interpolation filter. In addition to scaling, the video image may be cropped to an arbitrarily sized window.

Y/C Separation

Y/C separation involves extracting the luminance (Y) and the chrominance (C) components from the composite information. This is followed by quadrature demodulation to generate the baseband components (I and Q for NTSC or U and V for PAL) from the chrominance signal. The Bt835 implements an adaptive 2H comb filter to separate the chrominance from the luminance while maintaining full vertical resolution and eliminating “hanging dots” for the best possible NTSC Y/C separation. For PAL video, the Bt835 uses a notch/chroma comb filter. The Bt835 also provides hue, saturation, brightness and contrast controls which allow the user to adjust the decoded image‘s appearance.

Host Interface

Bt835 register access is implemented using I^2C, which is a serial two-wire interface (one data pin and one clock pin). The Bt835 behaves as an I^2C slave with a data transfer rate of 100 Kbps.

Data Sheet

You can obtain the data sheet and collateral information for the Bt835 from the technical document section on the Rastergraf web site.

5.12 Flash EEPROM

The graphics board has a 128 KB Flash EEPROM. It can be updated in the field using a special updater program. The code in the PROM cannot be directly executed by the CPU. It must be read by the host CPU into its memory and executed from there.

The SM731 accesses the PROM data through the SDRAM data port. The multiplexed address bits contain both the high and low order address lines for the PROM. The high order lines appear first and so must be latched externally.

Although in most cases the standard BIOS PROM would be 32 KB, a 128 KB is used on the Graphics board in order to accommodate multiple BIOS images (not currently implemented).

The way to go into the special PROM mode is this:

1) Program the SM731 chip to external bus, no refresh, mclk2 = 25MHz.

2) Read from prom location 0x990 (bits 12:4 = 0x99, rest don't care).

3) Read from prom location 0x660 (bits 12:4 = 0x66, rest don't care).

4) Set bit 3 at memory location 4 (bit 35 with dqm0 = false).

5) Write PROM address [16,1,0] at memory location 4 (with bit 3 set).

6) Read the PROM data.

7) To write PROM data, follow the memory location 4 write with a memory location 3 write of the data. The next PROM read will write the PROM with the data. To return to the read mode, write memory location 4 again.

8) To exit the special mode, clear bit 3 of memory location 4.

5.13 Serial EEPROM

The graphics board includes an IC position for an Atmel AT24C02 (or equivalent) 2 Kb (256 bytes) I^2C Serial Electrically Erasable Programmable Read Only Memory (EEPROM). The programming of the Serial EEPROM is done through secondary I2C control lines on the SM731.

Rastergraf reserves the first 128 bytes of the 256 byte Serial EEPROM for internal use. The remaining 128 bytes are left for user data. The use of the serial EEPROM on the graphics board does not currently have formal Rastergraf software support.

5.14 Interrupts

There is not a lot to say about interrupts for the graphics board. The SM731 chip is connected to the INTA line. The interrupt is controlled through the control registers in the chip itself. See ***Section 2.3.2*** for more comments about Interrupts. Note that if the LM75 Temperature Sensor is installed, it too can cause an interrupt on the INTA line.

What happens on that line at the other end (CPU side) is beyond the scope of this manual. In most cases, the interrupts are combined with other PCI slots, and the software will have to poll all PCI devices to see who made the interrupt.

Chapter 6
Troubleshooting

6.1 General Procedures

The boards were designed with reliability and durability in mind. Nevertheless, it may happen that a problem will occur. This section is devoted to aiding the user in tracking down the problem efficiently and quickly.

You may be able to locate minor problems without technical assistance. If the problem cannot be remedied, Rastergraf can then issue a Return Material Authorization (RMA) so that the board can be returned to the factory for quick repair.

It can happen that installing a new board will overload the computer's power supply if the power supply margins are exceeded. The first step in ascertaining if this is the problem is to calculate a power supply budget. This involves adding up the power requirements of each board in the system to see if you are within specification. Consult your computer's technical manual for information on how to correctly determine this. A typical board will draw a total of less than 1A total at +5V and +3.3V.

When attempting to verify that the power supply is working properly, it is not unusual to unplug everything and measure the supply without a load. While this practice is acceptable for linear supplies, switching supplies (which are very commonly used in computers) require a certain load before proper regulation is achieved. Typically, at least 4A must be drawn from the +5V supply before all the other voltages are properly regulated.

It can also happen that if you build your own cables and you short F5V on the front panel connector to ground you may trigger the auto-resetting fuse which protects power supply pins when an overload occurs. The fuse resets automatically when an overload is removed.

Note

If the board is not functioning, check that +3.3V is supplied on the host side connectors. The boards **REQUIRE** both +3.3V and +5V. The boards can be supplied with a local +3.3V regulator, so if there is no way to supply +3.3V on the backplane, there is a way out. Please contact Rastergraf if you need to do this. In addition, -12V is required for Sync-On-Green (SOG) to work correctly.

6.2 Dealing with the PCI Bus

Because of the nature of the PCI protocol and the way support has been implemented in the Operating Systems for PCI bus devices such as the graphics board , it is not possible to follow the same debugging strategies.

In fact, there are no address jumpers for these boards. Everything is configured in software through a set of on-board registers, which control the characteristics of the board as required by the PCI Specification.

The information used to program these registers is supplied to Operating System (OS) specific functions by Rastergraf' software. Ordinarily, several address map translations occur, including the CPU physical and virtual address maps and the CPU to PCI bridge address map.

While x86 systems generally follow the standards required to meet PC compatibility and mask these details, PowerPC systems do not. Among PowerPC vendors, there are no standards which ensure interoperability among CPU boards, even when they use the same CPU and PCI bridge.

Therefore, if you plan to use a graphics board in a PowerPC based system, it is vital to ensure that Rastergraf can vouch for the board's operation before you order the board. Otherwise, you may go crazy trying to figure out why it doesn't work. Please contact us (support@rastergraf.com or at (541) 923-5530 if you have problems.

6.3 Maintenance, Warranty, and Service

Maintenance

The graphics board requires no regular service, but if used in a particularly dirty environment, periodic cleaning with dry compressed air is recommended.

Because of the heat generated by normal operation of the graphics board and other boards in the system, forced crossflow ventilation ***is required***. If forced ventilation is not used, IC temperatures can rise to 60 degrees C or higher, which can cause premature product failure. With proper forced air-cooling IC temperatures will be less than 35 degrees C.

Warranty

The graphics boards are warranted to be free from defects in material or manufacture for a period of 12 months from date of shipment from the factory. Rastergraf' obligation under this warranty is limited to replacing or repairing (at its option) any board which is returned to the factory within this warranty period and is found by Rastergraf to be defective in proper usage. This warranty does not apply to modules which have been subjected to mechanical and/or electrical abuse, overheating, or other improper usage. This warranty is made in lieu of all other warranties expressed or implied. **All warranty repair work will be done at the Rastergraf factory.**

Return Policy

Before returning a module the customer must first request a Return Material Authorization (RMA) number from the factory. The RMA number must be enclosed with the module when it is packed for shipment. A written description of the trouble should also be included.

Customer should prepay shipping charges to the factory. Rastergraf will prepay return shipping charges to the customer. Repair work is normally done within ten working days from receipt of module.

Out of Warranty Service

Factory service is available for modules which are out of warranty or which have sustained damage making them ineligible for warranty repair. A flat fee will be charged for normal repairs and must be covered by a valid purchase order. If extensive repairs are required, Rastergraf will request authorization for an estimated time and materials charge. If replacement is required, additional authorization will be requested.

All repair work will be done at the Rastergraf factory in Redmond, Oregon, unless otherwise designated by Rastergraf.

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