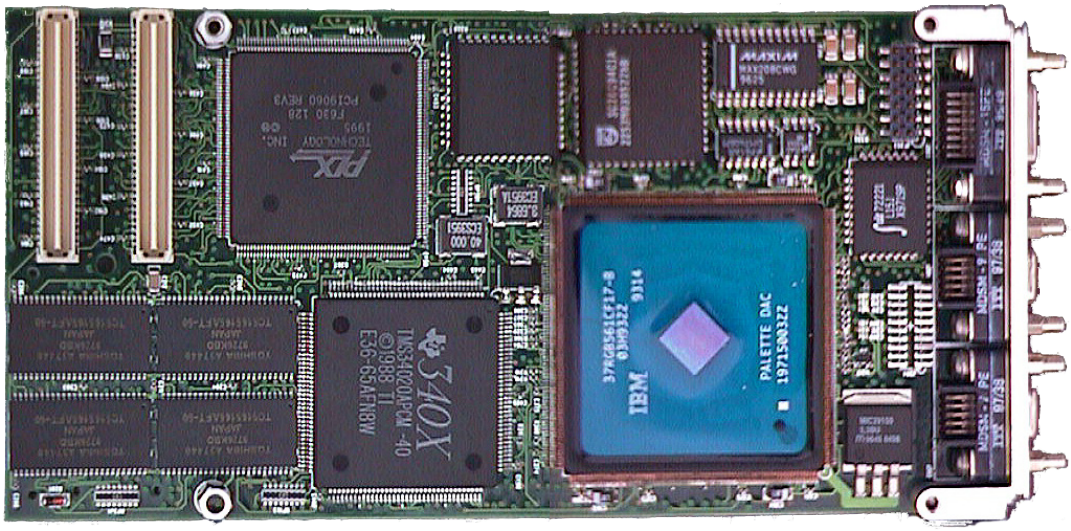
Rastergraf

VCL-M

High Resolution
Intelligent
PMC Graphics Controller



Features

- Intelligent graphics accelerator
- Up to 4 MB display memory
- Up to 32 MB processor memory
- Supports displays up to 1600 x 1200 at 8 bits/pixel
- True 8-bit overlay with independent color map
- On-board X Server available
- Two PS/2 ports and four RS-232 ports
- Suitable for non-VGA/Windows systems

The VCL-M

The Rastergraf VCL-M/8 is a single board 34020-based graphics display controller for PMC equipped VMEbus, CompactPCI, and other PMC/PCI Bus computers.

The VCL-M/8 includes an 8-bit overlay. The overlay screen can remain static while the primary scrolls (or vice versa).

The display memory which is used for the primary and overlay can be combined to support either primary-only double-buffered or high pixel count (e.g. 2048 x 1536) displays.

The 40 MHz TMS 34020 32-bit Graphics System Processor draws random points at a 10 Megapixel per second rate, and normal pixblt, pattern fills, and vector generation at up to 40 Mpix/sec rate. Hardware acceleration features include color and writemask registers, VFILL, and VBLT, and can give up to 160 Mpix/sec on a block write.

The 34020 can receive interrupts from the PMC Bus, serial I/O, and vertical sync. It controls the video timing, supporting almost any screen resolution from 256 pixels to 2048 pixels, at 30 to 80 Hz vertical and 15.7 to 100 KHz horizontal refresh rates. Standard display formats range from 640 x 480 to 1600 x 1280. Interlaced and non-interlaced formats are supported. A PLL clock generator allows the user to change the pixel clock.

The VCL-M supports binary vertical zoom (1,2,4,8,16), non-integer horizontal zoom (by virtue of the PLL pixel clock), horizontal pan and vertical smooth scroll.

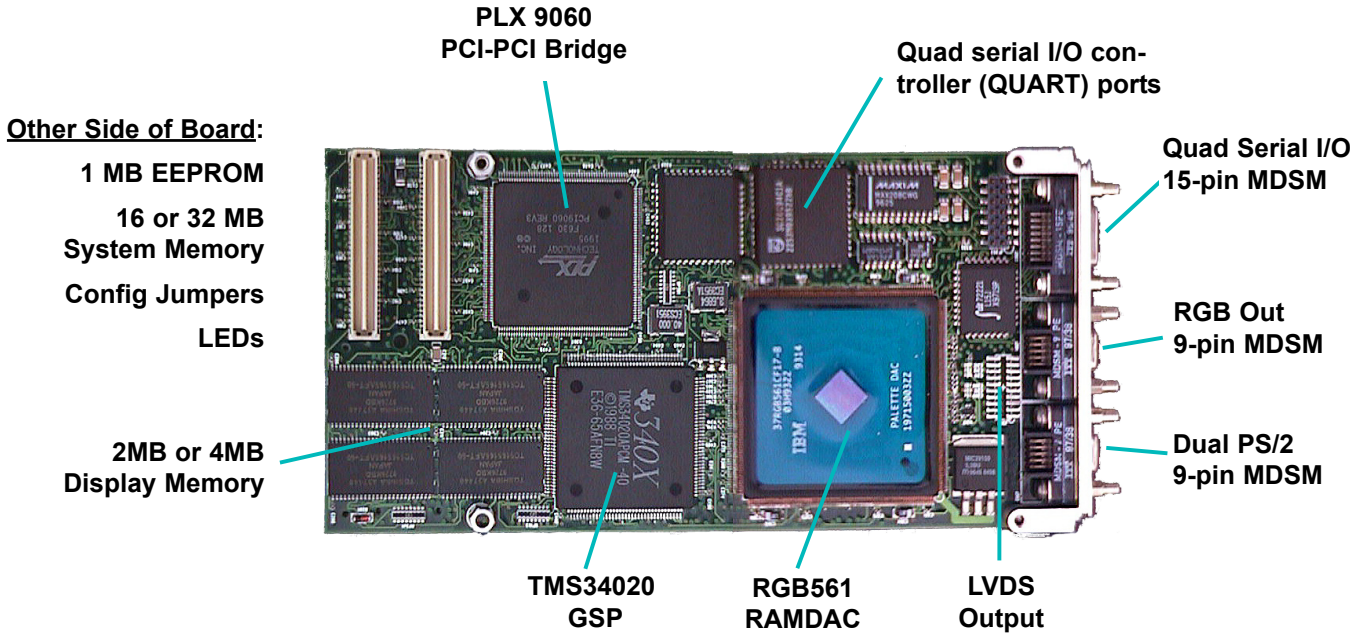
The display memory uses VRAMs, which gives about 95% availability to the 34020 and host processors. The display size ranges from 1 million up to 4 million addressable pixels.

The video output is directed through an IBM RGB561 RAMDAC. The 561 supports simultaneous analog and digital output. It includes a graphics cursor with a 64 x 64 x 2 bit map. It translates the primary, overlay, and 2-bit cursor pixels into 24-bit color values (8 bits each of red, green, and blue). The output can optionally be passed through a 10-bit/color Gamma correction table. The analog red, green, and blue signals from the color map are connected to a standard RGB monitor.

The optional FPD/LVDS compatible digital video output port supports most flat panels up to 1280 x 1024 resolution. Pixel output is either two 12-bit (4 bits each RGB) or one 24-bit (8 bits each RGB) per clock.

The VCL-M/8 front panel has three micro D-Sub connnectors, which provide analog video, two PS/2 (PC) and four RS-232 serial ports (for mouse, trackball, touchscreen, console, etc.).

Please note that the VCL-M/8 is not supported under Windows and is not VGA compatible.



VCL-M Features

- Complete intelligent graphics controller on a single PMC
- High performance TMS34020 32-bit graphics processor
- 16 or 32 MB of 34020 system memory
- VRAM/Hardware Pixel Acceleration
- Independent Overlay and Primary screen positioning
- Analog output up to 2048 x 1536
- LVDS Digital output up to 1280 x 1024
- 2M pixels each of primary & overlay or 4M pixels of primary
- 10-bit gamma correction
- 4 serial ports + 2 PS/2 (PC) ports
- 1 MB Flash PROM
- 33 MHz, 32-bit PCI interface
- Can run autonomous X Server, Graphics Package, or other customer-supplied code.

VCL-M Technical Overview

The VCL-M/8 is designed as an autonomous subsystem with links to the PMC bus. Using the intelligence of the onboard TMS34020, programs as sophisticated as X Windows can be run on-board with a minimum of support from the host CPU. The local 1 MB flash is sufficient to store an entire server, including some local fonts, or, alternatively, the CLP graphics library package and SmatPTERM, the terminal emulator.

PMC Bus Interface uses a PLX9060 PCI bridge for the interface to the VCL core logic. The 9060 has transmit/receive FIFOs, programmable address, interrupt, and control registers and a high performance DMA channel. The 9060 also controls two VCL-M/8 local registers which contain the Control Status Register (CSR) and the Line Address Register (LAR).The 16-bit LAR selects device registers (34020, color map, serial I/O) or a part of VCL-M/8 memory for access through the PMC bus address windows.

The VCL-M/8 uses the 40 MHz TMS 34020 Graphics Processor, which has a complete instruction set 32-bit CPU, vector and pixblt functions, writemask register, and programmable video timing. Note: due to space constraints, the VCL-M/8 does not support the 34082 FPU Coprocessor.

34020 system memory includes 1 MB of 32-bit wide Flash EEPROM, suitable for direct program execution, 16 or 32 MB of 0-wait-state DRAM for programs and off-screen data, 4 Kb of serial EEPROM for power-up parameter storage. Display memory consists of 2MB or 4 MB VRAM, which can be arranged as primary and overlay (2 Mpix each) or primary-only configuration (4 Mpix). Maximum display format is 1600x1200.

Hardware Scroll, Pan, and Zoom is supported as single line (smooth scroll), pan is programmable on 4 pixel boundaries, and zoom (vertical: 1,2,4,8,16). Overlay and Primary displays can be independently panned and scrolled.

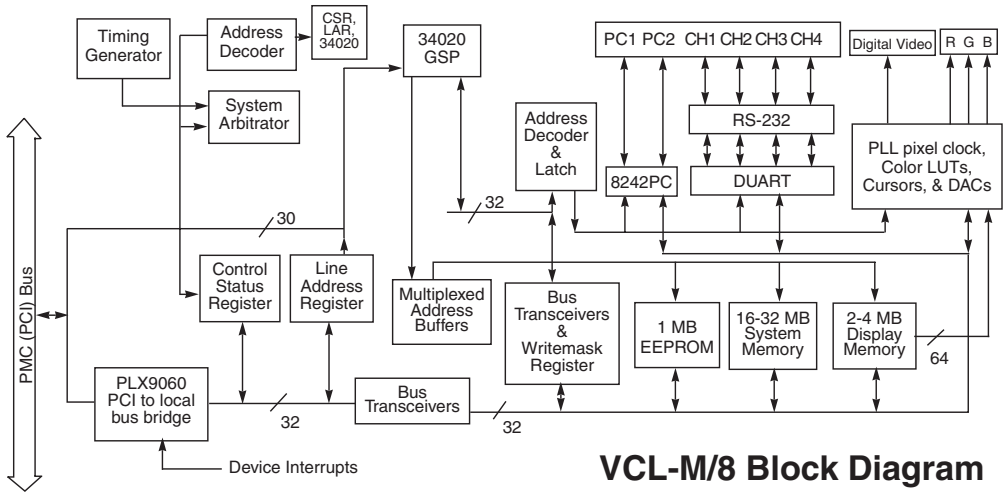
34020 can interrrupt the PMC Bus via the PLX9060 bridge chip.

The IBM RGB561 Analog and Digital color map includes a 2 bit 64 x 64 bit map/crosshair cursor, 10-bit DACs and 10-bit Gamma correction table. Interlaced and noninterlaced displays are supported. The VCL-M/8 uses the RGB561 as an 18-bit in (8 bit overlay, 8 bit primary, 2 bit cursor) 24-bit out (8 bits each red, green, blue) look-up table.

Digital output can be configured to output one 24-bit RGB pixel or two 12-bit RGB pixels. The two pixel mode is compatible with high resolution flat panels. The pixel value can also be mapped to one 8-bit gray-scale pixel, two 4-bit gray scale pixels, or eight 1-bit pixels. The digital output is encoded in the National FPD/LVDS high speed output system.

The VCL-M has two PS/2 (PC) compatible ports with TTL data/clock composite ports contained in an Intel 8242PC. It also has four RS-232 serial channels, contained in a SC26C94 QUART. Each channel has a 4 byte receive FIFO and programmable baud rates up to 38.4 Kbaud. The QUART has two timer/counters and control bits that drive 3 status LEDs.

Console - female DB-9 with RX, TX, CTS, RTS, and ground. CTS and RTS can be reassigned to make another serial port. Primary and Secondary Serial Ports can be used for serial type PC mouse, trackball, and/or touchscreen.



VCL-M/8 Block Diagram

VCL-M Software

Software support is available for Unix and most real time operating systems and includes:

+ **X Windows X11R6 Server** is board based for best performance. Includes extensions for overlays, multiple input devices, direct access to display memory, and fast vector generation.
+ **CLP Graphics Subroutine Package** provides low overhead access to the VCL-M through calling sequences to an on-board subroutine set.
+ **C compiler toolset** for user written 34020 applications.
+ **SmartPTERM -** is an **Open Firmware Monitor and BIST System.** It is a Flash-based auto-booting monitor that provides Built In Self Test (BIST), front panel LED diagnostics, and can boot to **PTERM** (a simple ***vi*** compatible terminal emulator), **CLP**, or **PX Windows** ROM images (included). **SmartPTERM** can store and modify initialization tables and configuration data in the VCL-M/8's Serial EEPROM.

VCL-M Product Specifications

Graphics Controller	TI TMS34020-40
Maximum Dot Clock	170 MHz
Horizontal Scan Rates	31.5 to 115 KHz
Display Resolution	1600 x 1200 (max.)
Display Colors	256 from 24-bit (16.7M color) LUT
Memory Configuration	
Display memory	2MB or 4MB VRAM
System memory	16MB or 32 MB DRAM
32-bit Flash memory	1MB
Serial EEPROM	4Kb
Analog Monitor Support	Multi-frequency (VGA type) or composite-RGB, interlaced or non-interlaced. Sync-On-Green is software selectable.
Composite Video/Sync Signal	1 Volt peak to peak, consisting of: 660 mV Reference White 54 mV Reference Black 286 mV Sync (Sync on Green)
Flatpanel Support	FDP/LVDS encoded digital output, vertical and horizontal sync, clock, and blanking.
PCI-PCI Bridge	33 MHz PLX9060 PCI-to-Local Bridge. Supports extended burst cycles and automatic bus retry.
PMC Bus Compatibility	IEEE P1386.1 and PCI 2.1 compliant 32-bit (J1 only)
Front Panel Connections	
Analog Output Connector	9-pin Cannon MDSM Micro D-sub
Digital Video Connector	20 pin ribbon connector behind front panel.
Dual PS/2 Port Connector	9-pin Cannon MDSM Micro D-sub
Quad RS-232 Connector	15-pin Cannon MDSM Micro D-sub
Adapter cables	
MVI-2/2	MDSM-9 to VGA Breakout Cable
MSE-2/2	MDSM-9 to dual DB9 Breakout Cable. "Console" is female DB-9 with RX, TX, CTS, RTS, and ground. CTS and RTS can be used make another serial port. "Secondary" is RX, TX only.
MKM-2/2	MDSM-9 to PS/2 Breakout Cable splits out the mouse and keyboard to PS/2 mini-DIN.
Software Support	Linux/XFree86 and VxWorks DDX CLP Graphics for VxWorks Flash-based SmartPTERM, CLP, and PX Windows Server options are available.
Multiple Display Support	Multiple VCL-M boards may be added to a single system.
VCL-M Maintenance Features	Red, Amber, and Green LEDs can be used for diagnostics by customer software. The RGB561 can report valid monitor connections.
Environment	
Operating temperature	0°C to +70°C
Storage temperature	-55°C to +85°C
Humidity	10% - 90% non-condensing
Power Requirements	+5V ±5%, 1.5 A typical
Dimensions	IEEE 1386 PMC, 149mm x 74mm

Display Resolutions

Resolution	Vertical Scan Rate		Primary/ Overlay
	Unix and RTOS		
	Format	Frequency	
640 x 480	VGA	60 Hz 75 Hz	both
800 x 600	SVGA	60 Hz 75 Hz	both
1024 x 768	UVGA	60 Hz 75 Hz	both
1152 x 864	Sun	60 Hz 75 Hz	both
1280 x 1024	SXGA	60 Hz 75 Hz	both
1600 x 1200	UXGA	60 Hz	Primary only

Ordering Information

VCL-M/8

The VCL-M includes 40 MHz TMS 34020 Graphics Processor, 16-32 MB 34020 memory, hardware pan, scroll, and zoom, 2-bit cursor, and analog and (optional) digital output, 4 RS-232 serial ports and 2 PS/2 ports.
Note: digital display option cannot exceed 1280 x 1024.

Model	Typical Display	34020 Memory	X Compatible	Overlay	1 MB Flash	Digital Out
VCL-M/8/X10	1024 x 768	16 MB	yes	yes	yes	no
VCL-M/8/X12	1280 x 1024	16 MB	yes	yes	yes	no
VCL-M/8/X16	1600 x 1200	16 MB	yes	no	yes	no

Transition Cable Assembly:

MVI-2/2 MDSM-9 to VGA Breakout Cable

MSE-2/2 MDSM-9 to dual DB9 Breakout Cable

MKM-2/2 MDSM-9 to PS/2 Breakout Cable.

Software:

Unix and VxWorks CLP and PxWindows drivers are available. Please contact the factory for more information.

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