VFX-M

Graphics Board User's Manual

Rastergraf

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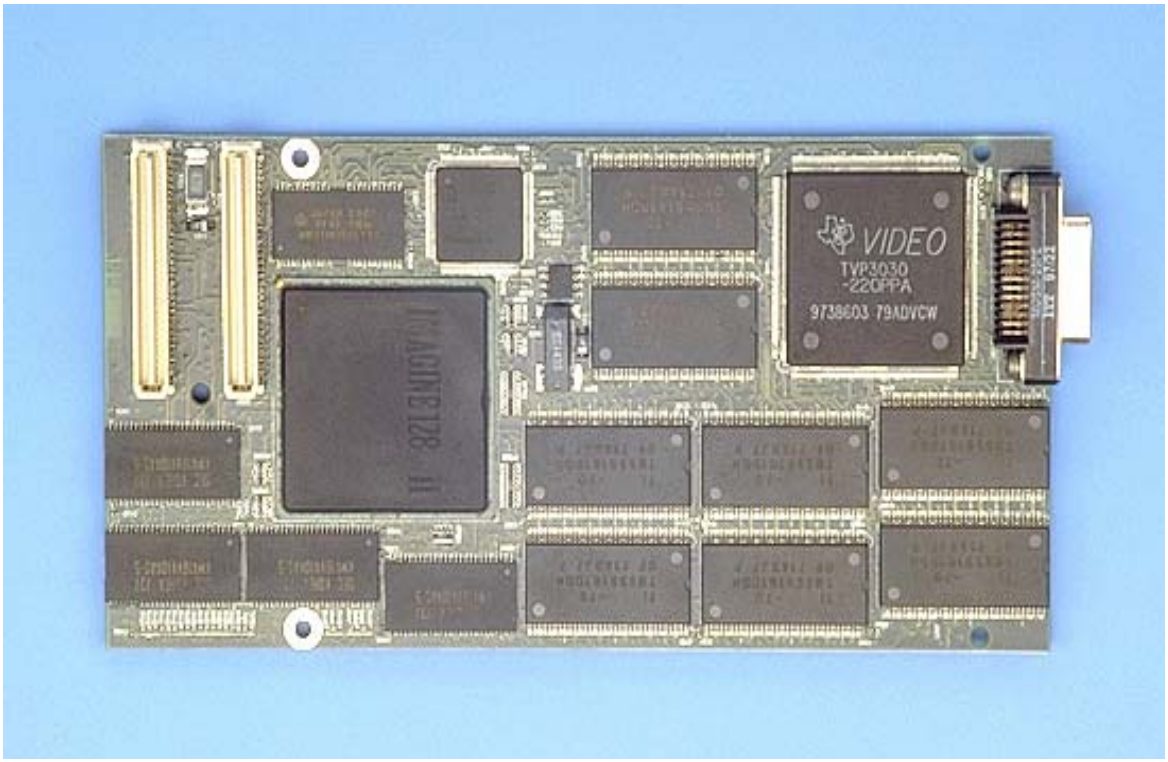


Introduction

This manual provides information about how to configure, install, and program the Rastergraf VFX-M PMC (**P**CI **M**ezzanine **C**ard) graphics controller, which uses the Number Nine I128S2 graphics controller chip.

This manual is broken down into five chapters:

Chapter 1: Overview of the VFX-M
Chapter 2: Installing VFX-M
Chapter 3: Summary of Rastergraf's Software Products
Chapter 4: Programming VFX-M Devices and Memories
Chapter 5: Troubleshooting

Chapter 1 provides background material about VFX-M graphics boards. Understanding the information in the chapter, however, is not essential for the hardware or software installation. If you want to perform the installation as quickly as possible, start with Chapter 2. If you have problems installing the hardware, refer to Chapter 5 for help.

Getting Help

This installation manual gives specific steps to take to install your Rastergraf display board. There are, however, variables specific to your computer configuration and monitor that this manual cannot address. Normally, the default values given in this manual will work. If you have trouble installing or configuring your system, first read Chapter 5, "Troubleshooting". If this information does not enable you to solve your problems, do one of the following:

1) call Rastergraf technical support at (541) 923-5530,

2) fax your questions to (541) 923-6475,

3) or send E-mail to ***support@rastergraf.com***.

If your problem is monitor related, Rastergraf technical support will need detailed information about your monitor.

Board Revisions

This manual applies to the following board revision levels:

VFX-M Fab Rev 0, 1

Notices

Information contained in this manual is disclosed in confidence and may not be duplicated in full or in part by any person without prior approval of Rastergraf, Inc.. Its sole purpose is to provide the user with adequately detailed documentation to effectively install and operate the equipment supplied. The use of this document for any other purpose is specifically prohibited.

The information in this document is subject to change without notice. The specifications of the VCQ-M, VFG-M, and other components described in this manual are subject to change without notice. Although it regrets them, Rastergraf, Inc. assumes no responsibility for any errors or omissions that may occur in this manual.

Rastergraf, Inc. assumes no responsibility for the use or reliability of software or hardware that is not supplied by Rastergraf, or which has not been installed in accordance with this manual.

Trademarks mentioned in this manual are the property of their respective owners.

The VFX-M is manufactured and sold under license from Curtiss-Wright Controls Embedded Computing. Contact Rastergraf, Inc. for additional information.

Manual Revisions

Revision 0.1	September 25, 1998	New
Revision 0.2	January 15, 1999	Cleanup and revisions
Revision 1.0	March 19, 1999	First released version
Revision 2.0	October 24, 2006	Revised for Rastergraf version. Delete the PS/2 ports

Conventions Used In This Manual

The following list summarizes the conventions used throughout this manual.

`Code fragments`	Code fragments, file, directory or path names and user/computer dialogs in the manual are presented in the `courier` typeface.
Commands or **program names**	Commands, or the names of executable programs, except those in code fragments, are in bold.
System prompts and commands	Commands in code fragments are preceded by the system prompt, a percentage sign (%), the standard prompt in UNIX's C shell, a dollar sign ($), the OS-9 prompt, or the hash-mark (#), the standard UNIX prompt for the Super-User.
Keyboard usage	**<CR>** stands for the key on your keyboard labeled "RETURN" or "ENTER"

Note	Note boxes contain information either specific to one or more platforms, or interesting, background information that is not essential to the installation.

Caution	Caution boxes warn you about actions that can cause damage to your computer or its software.

Warning!	Warning! boxes warn you about actions that can cause bodily or emotional harm.

Chapter 1
General Information

1.1 Introduction

The Rastergraf **VFX-M** is part of Rastergraf's new series of single PMC modules designed to provide unique functions to the user. The VFX-M joins the **VCQ-M**, a high integration, high performance 2D four channel graphics controller, and the **VCL-M**, a high resolution, medium performance graphics controller which is derived from the VCL-V VMEbus graphics board. More information about Rastergraf's products can be obtained by contacting the factory or consulting Rastergraf's web page at http://www.peritek.com.

This chapter provides an overview of the VFX-M graphics controller. Additional sections contain a bibliography, specifications, monitor requirements, and common configurations. Installation procedures are contained in Chapter 2.

The Rastergraf **VFX-M** is a single board PMC graphics display controller for VMEbus and CompactPCI computers. It has a Number Nine Imagine 128 Series 2 (I128S2) UVGA compatible 128-bit graphics accelerator. The VFX-M can function as the system VGA controller and includes an on-board BIOS PROM.

The VFX-M can be used on a standard PCI bus machine by plugging it into a PMC to PCI adapter board.

1.2 Functional Description

As an aid to understanding the VFX-M, a block diagram is provided at the end of this section. The feature set of the VFX-M includes:

- 128-bit 50 MHz Number Nine Graphics Controller
- Embedded VGA controller and BIOS
- 2 Kb serial EEPROM
- 128 KB Flash PROM
- 64 MB Pixmap memory
- Better than 1600 x 1280 displayable analog resolution
- 8-bit overlay (when running 16 or 32 bpp display)
- 8 MB high speed VRAM supports multiple display pages
- 2 MB high speed DRAM supports bit-mapped mask buffer
- Hardware pan, zoom, and scroll and bitmapped cursors
- PLL controlled pixel and memory clocks
- Non-interlaced, interlaced, and high refresh rate displays
- Three status LEDs (controlled by host software)
- Single 25-pin Cannon Micro D-Sub supplies RGB and Serial I/O
- PMC single-wide module
- Ruggedized version (contact Rastergraf for availability)
- OpenGL Library
- Graphics Subroutine Package
- X11R6 X Window System Server with GLX (OpenGL extensions)
- X Windows and Windows NT build options

The ***Imagine 128 Series 2*** (I128S2) is a 128-bit graphics controller with accelerated 2D and 3D patterned lines and shaded triangles, Z buffer, and 3D volume clipping. It provides a high performance PCI 2.1 compliant interface with no additional external logic required.

The I128S2 is implemented using a Symmetric Multi-Graphic Processor (SMGP) architecture. This architecture allows the execution of two drawing commands simultaneously with totally independent parameters. The **Drawing Engine** commands provide all of the normally required operations including: BitBLT, Line, Triangle, Write Image, and Read Image. Software may interact with the I128S2 by directly manipulating pixels through the Memory Windows interface. A secondary **Copy Engine** can be used to independently move pixmaps from one memory area to another.

The I128S2 is implemented in a 0.5 micron 3.3 volt CMOS gate array process and is packaged in a 352 PBGA, (Plastic Ball Grid Array).

Key I128S2 Device Features:

- 33 MHz PCI 2.1 host interface clock
- Asynchronous graphic processor
- EDO Memory controller supports high speed image transfer
- Integrated VGA
- Independent Drawing and Copy Engines
- Integrated display list processor
- Integrated display controller
- Integrated Color space converter
- Directly supports 8, 16, 32 bpp
- Two Operand BitBLT
- Scaling with X and Y interpolation
- Flat and shaded line drawing with patterning
- Flat and Gouraud shaded patterned triangles
- Shared Z buffer, frame buffer, and back buffer
- Hardware three dimensional volume clipping
- 16-bit logical addressing in both X and Y, and 32-bits in Z
- One XY and Two Linear Memory Windows
- Interrupts from the raster line counter and the drawing completion

The VFX-M can address 8 MB of VRAM Display Memory, 2 MB of Mask Buffer DRAM, and 64 MB Pixmap Memory.

Important Note

Note that because the Windows driver doesn't use them, the Mask Buffer and Pixmap Memories are not included in the VFX-M/NT build version.

The VFX-M display memory data is directed to the monitor via a Texas Instruments TVP3030 RAMDAC color map control chip which provides a single programmable 24 bit wide color map (8 bits each red, green, and blue) The TVP3030 also provides VGA compatibility, overlay screen, PLL pixel clocks, and a two bit cursor with a 64 x 64 x 2 bit map.

Programmable timing and control registers control the video timing. Both interlaced and non-interlaced formats are supported. A programmable clock generator allows the user to change the pixel clock. Display formats range from 640 x 480 to better than 1600 x 1280 x 32 bpp.

All connections are made through the front panel 25-pin Micro D-Sub connector. A special breakout cable assembly converts the monitor (analog RGB and sync), and DDC functions into a VGA-style connector.

Rastergraf software support is available for most operating systems and includes:

Graphics Library Package: **GLP** is a complete Graphic Subroutine Library with direct (non-X) OpenGL compatible extensions.

Windows NT/2K Drivers.

PC Compatible Video BIOS: provides PC for use in x86 or x86 BIOS emulating systems.

X Windows X11R6 Solaris and Linux Servers (contact Rastergraf for availability): **PX Windows** is optimized for the I128S2 graphics accelerator.

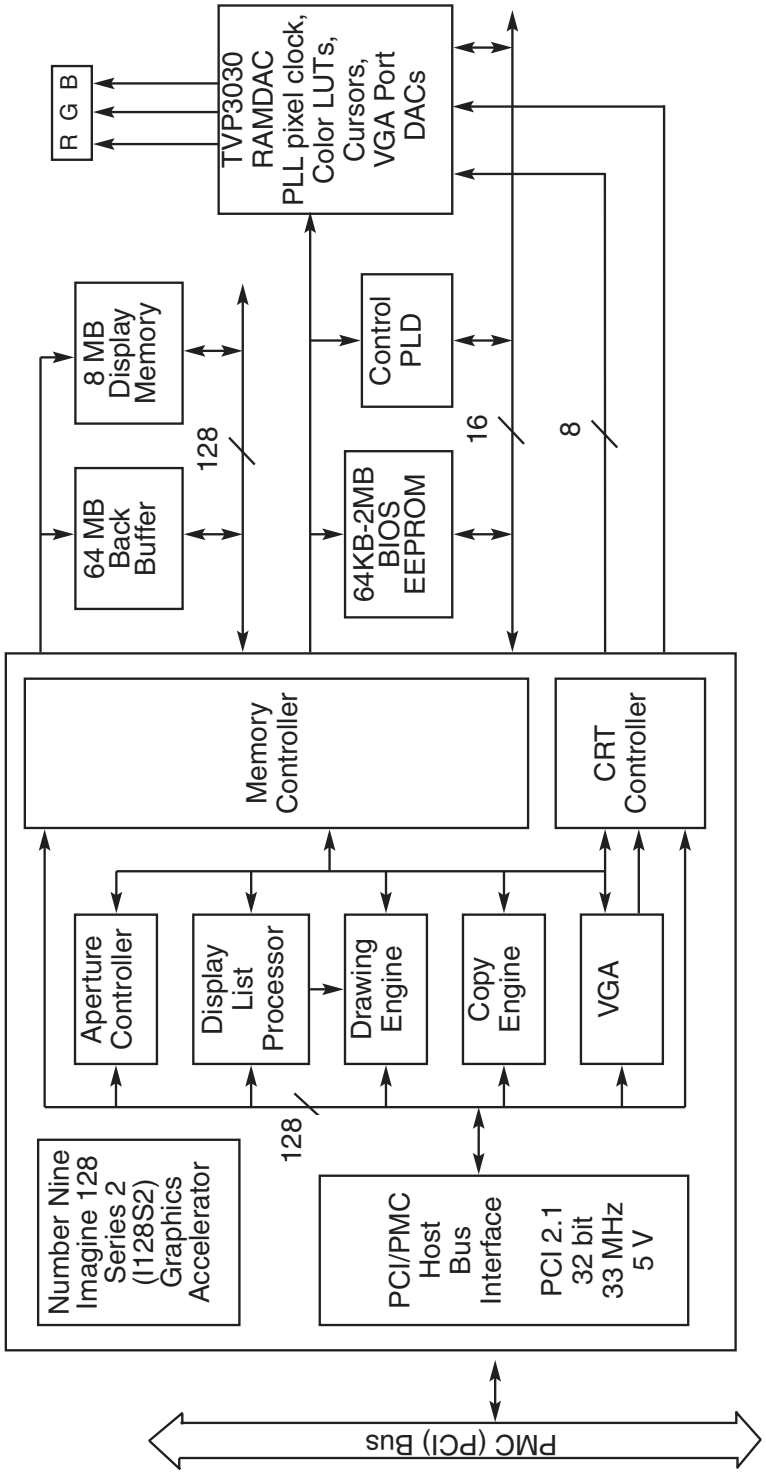


Figure 1-1 VFX-M Block Diagram

1.3 Additional References

Rastergraf documentation includes User's Manuals, Graphics Library Package Manual, and Rastergraf PX Windows Server Installation and User's Guide. Rastergraf includes on its Software Distribution CD a set of Technical Libraries which includes a lot of chip specific data:

Rastergraf Software CD
Device Specific Technical Archives

Rastergraf Inc.
1804-P SE First Street
Redmond, OR 97756
(541) 923-5530

Number Nine Imagine 128 Series 2 Technical Manual
This is available from Rastergraf once a Non-Disclosure Agreement (NDA) has been executed or web-page password has been granted.

TVP3030 Data Sheet
Order # SLAS111

Texas Instruments
Customer Response Center
1-800-232-3200
http://www.ti.com/sc/docs/folders/analog/tvp3030.html

PCI Local Bus 2.1 Specification

PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177

Graphics Textbooks

Fundamentals of Interactive Computer Graphics
Addison Wesley, 1993. Foley and Van Dam

Principles of Interactive Computer Graphics
McGraw-Hill, 1979 Newman and Sproull

1.4 General Specifications for the VFX-M

Graphics Processor: 50 MHz Number Nine I128S2 High Performance 128-Bit Graphics and Multimedia Processor. Has a 128-bit vector and pix-blt functions and programmable video timing. The I128S2 provides support for VRAM color and write-per-bit register special functions.

The maximum supported frequencies are 220 MHz for the pixel clock and 100 MHz for the memory clock.

Display Memory (VRAM): The VFX-M display memory 128-bits/word, byte addressable, no-wait state, dual-port VRAM

The small size of the VFX-M limits the choice of display memory (VRAM) to either 4 MB or 8 MB. The standard VFX-M is built with 8 MB, as this provides the greatest flexibility. However, the 4 MB version is available by special order.

8 MB of VRAM gives five pages of 1600 x 1280 using 8-bit pixels, two pages using 16-bit pixels, or one page using 32 bpp.

Pixmap Memory (DRAM): Memory is 64 MB of 128-bits/word, byte addressable, no-wait state, dynamic RAM. This memory is in the same memory space as the display memory, so it can hold program store and pixmap display data.

In the case of DRAM, there are two choices of DRAM size: all or nothing: Giving up the DRAM can save significant cost, but for X Windows applications (especially) you will suffer a significant loss of performance.

EEPROM Memory: One 8-bit Flash EEPROM supports a 128 KB 8-bit wide permanent storage. Normally, it is programmed with a VGA BIOS.

A 2 KBit (256 byte) serial EEPROM, programmed via I128S2 DDC control lines, supplies non-volatile read-mostly memory to retain some changeable data during power down.

.

Video Display: The Texas Instrument TVP3030 color lookup table (CLUT) resolves the display priority between the primary, overlay, and cursor (last through first, respectively) screens.

For 8-bit applications, the pixel size is 8 bits, and there is 1 byte per pixel. For 16 and 32 bit applications the pixel is divided into Red, Green, and Blue components. A color key can be used to switch the TVP3030 from passing the RGB components straight through to sampling the pixel to the color map, thus providing a mapped overlay value.

Pixel Clock: The TVP3030 RAMDAC contains a programmable pixel clock generator. This allows the pixel clock to be set to virtually any frequency between 5 and 250 MHz. The upper range can be extended to 270 MHz by special order.

Scroll, Pan, and Zoom: Scroll - single line (smooth scroll).
Pan - anywhere on 16 byte boundaries
Zoom: vertical (incremental)
horizontal: sub-integer, uses the TVP3030 PLL to adjust master pixel clock.

Color Map: The VFX-M video output uses a TI TVP3030. The input multiplexer can be programmed to correspond to the pixel size of 8, 16, or 32-bpp by operating in 16:1, 8:1 or 4:1 (respectively) mux mode.

It supports VGA and common interlaced and non-interlaced displays ranging from 640 x 480 up to better than 1600 x 1280. The TVP3030 has a 64 x 64 x 2 bitmapped cursor. The DAC outputs are 8-bits.

PMC (PCI) Bus Access: All VFX-M registers and memory are accessible to the PCI bus through the I128S2's integral PCI bus bridge. The I128S2 provides programmable Bus Address Registers (BARs) that map control registers, drawing engine registers, and memories. A 16 MB memory-mapped windows gives direct access to VRAM, while a 32 MB window enable access to one-half of the 64 MB pixmap memory.

PCI bus Interrupts: The I128S2 can cause an interrupt on the INTA line.

Bus Loading: One PCI 2.1 compatible load

Front Panel Connections: The VFX-M has a single 25-pin Cannon MDSM micro D-Sub connector on the front panel.

Breakout Cable: Rastergraf can provide a front panel breakout cable to supply Red, Green with Composite Sync, Blue, and TTL level DDC, horizontal and vertical sync on a VGA compatible connector.

Module Size: Standard IEEE 1386 PMC bus card, 149 mm x 74 mm. .

PCI Subsystem Vendor ID: 0x10F0 (Rastergraf Vendor Code)

PCI Subsystem Device ID: 0x001F for VFX-M Rev 0, 0x0000 for VFX-M Rev 1

Power Requirements: +5V +/- 5%, 1.5 A typical.

Environment:

Temperature:	0 to 70 degrees C, operating
	-55 to +85 degrees C, storage
Humidity:	10% to 90%, non-condensing

Ruggedization Option: Although Rastergraf is not formally in the militarized business, it does offer a "ruggedized" version of the VFX-M. ***Commercial grade components are used.*** The board is protected with a conformal coating. It is Miller Stephenson MS-460A spray-on, and is MIL-I-46058C, Type SR and MIL-T-152B compliant. The board is tested under extended temperature conditions:

Temperature:	-20 to 80 degrees C, operating
	-55 to +85 degrees C, storage

1.5 Monitor Requirements

Rastergraf display boards can be used with a wide variety of monitors. For best performance a monitor should have the following features:

- VGA compatible 5 Wire RGB with separate TTL horizontal and vertical sync or 3 Wire RGB with sync on green (see note below)
- Switchable Termination (for monitor loopthrough)
- Height, pincushion, width, phase, and position controls
- Autotracking horizontal and vertical synchronization
- High bandwidth: 135 MHz at 1280 x 1024
  180 MHz at 1600 x 1280
- Horizontal refresh rate: 70 kHz at 1280 x 1024
  90 kHz at 1600 x 1280

Note

A standard Multiscan monitor can be plugged directly into the VFX-M's adapter cable using a VGA cable with 15 pin D-Sub ends. However, in order to avoid a green background, select **NO SYNC ON GREEN** when setting up the VFX-M's Video Parameters.

Table 1-1 VFX-M Standard Display Timing Specifications

Display Format	Vertical Refresh	Horizontal Refresh	Pixel Clock
640 x 480	60 Hz	31.5 kHz	27 MHz
1024 x 768	60 Hz	60 kHz	80 MHz
1024 x 1024	70 Hz	64 kHz	85 MHz
1280 x 1024	60 Hz	64 kHz	110 MHz
1280 x 1024	67 Hz	72 kHz	125 MHz
1600 x 1280	60 Hz	79 kHz	170 MHz

Composite Video Signal: 1 Volt peak to peak consisting of:
660 mV Reference White +
54 mV Reference Black +
286 mV Sync Level

1.6 Configuration Information

The basic graphics board includes:

- 50 MHz Number Nine Graphics Processor
- hardware cursors
- hardware pan, scroll, and zoom
- programmable pixel clock
- analog video outputs
- interrupts
- VGA BIOS
- 2 Kbit serial EEPROM
- 3 diagnostic LEDs

Please contact Rastergraf and/or refer to the short form catalog for more information about configurations and accessories. The following tables show some common models.

Table 1-2 Common VFX-M Configurations

Model	Video Memory	Pixmap Memory	Software Compatibility	Display Format	Pixel Size
VFX-M/X	8 MB	64 MB	**PX, GLP, WN**	1600 x 1024	8,16,32
VFX-M/L	8 MB	0	**PX, GLP, WN**	1600 x 1280	8,16,32
VFX-M/LC	4 MB	0	**PX, GLP, WN**	1600 x 1280	8

Note: **PX** means PX Windows,
GLP means Graphics Library Package, and
WN means Microsoft Windows NT native drivers.

Chapter 2
Installing Your Rastergraf Graphics Board

2.1 Introduction

There are 2 steps involved in getting your Rastergraf Display board to work in your system:

- Unpack and install the Rastergraf display board.
- Install the software

This chapter shows you how to install the Rastergraf display board in your computer. Your Rastergraf software User's Manual (e.g. GLP) provides instructions on how to install the software.

2.2 Unpacking Your Board

When you unpack your board, inspect the contents to see if any damage occurred in shipping. If there has been physical damage, file a claim with the carrier at once and contact Rastergraf for information regarding repair or replacement. Do not attempt to use damaged equipment.

> **Caution**
>
> Be careful not to remove the board from its antistatic bag until you are ready to install it. It is preferable to wear a grounded wrist strap whenever handling computer boards.

Some operating systems require that you reboot your system after installing a device driver, because only after the reboot will your system utilize the driver and recognize the board. If yours is such an operating system, you might like to install your Rastergraf software **before** installing the board since you will have to shut down the computer to install the board anyway. If you want to install the software before shutting down the computer, proceed to the correct part of the relevant software manual and return to this chapter afterwards.

2.3 VFX-M Installation

The VFX-M is designed to plug into any IEEE 1386 compatible single module PMC location. PMC locations are currently supported on VME and CompactPCI compatible computers and PCI/PMC expander boards.

The VFX-M will also work correctly in a system where the base board is a PCI motherboard. In this case, you can use a Rastergraf **PMA-P** PMC to PCI adapter to enable plugging a PMC board (the VFX-M) into a PCI slot. Although perhaps not suitable for a long term installation, it can be a convenient thing to do.

2.3.1 Address Settings for the VFX-M

Since the PCI bus and the VFX-M are configured by the operating system and/or BIOS while booting up, there aren't any address jumpers. The address settings are programmable and are set up by the VFX-M software as a result of information supplied by the OS at boot time. Refer to the Rastergraf software User's Manuals for more information.

The Rastergraf VFX-M uses registers in the Number Nine I128S2 Graphics Processor chip internal register set and also sets up address ranges outside the I128S2's (internal) address space which give access to the VFX-M's control registers, RAMDAC, and memory blocks. The BAR (Base Address Register) sets in the I128S2 are programmed to point to these areas.

The Rastergraf VFX-M device driver will load the BARs if the O/S or BIOS did not. If you can determine the actual PCI base address, you might even be able to probe the address spaces with an on-line debugger once the driver code has run. Section 4.3 has details on how the I128S2 controls access to the on-board registers.

You will notice that there isn't any good information supplied here which will allow you to reliably probe the VFX-M addresses. That is because the ability to do this is absolutely dependent on the CPU board memory map as implemented by the system OS and the address ranges of the PCI bus as determined by the CPU hardware. These things change from OS to OS, board to board, and vendor to vendor, making this a difficult task.

Therefore, you have to work closely with your CPU board, the OS's BSP, and collateral information supplied by Rastergraf to actually touch the registers. Most likely, if you use Rastergraf supplied software, the board will show up and you will get pictures.

2.3.2 Default Interrupt Settings on the VFX-M

The VFX-M is hard-wired for PCI/PMC interrupt request INTA. Since each PMC slot maps its interrupt lines to a permuted set of INTA-INTD, the VFX-M will show up on a different interrupt line, according to the slot it is plugged into. Thus, the device driver may need to be changed to reflect this. The VFX-M has a interrupt response is controlled by the Rastergraf device driver.

2.3.3 Installing the Graphics Board

Use the following procedure to install the VFX-M into the computer

1. Shut down the operating system and **turn off the power**.

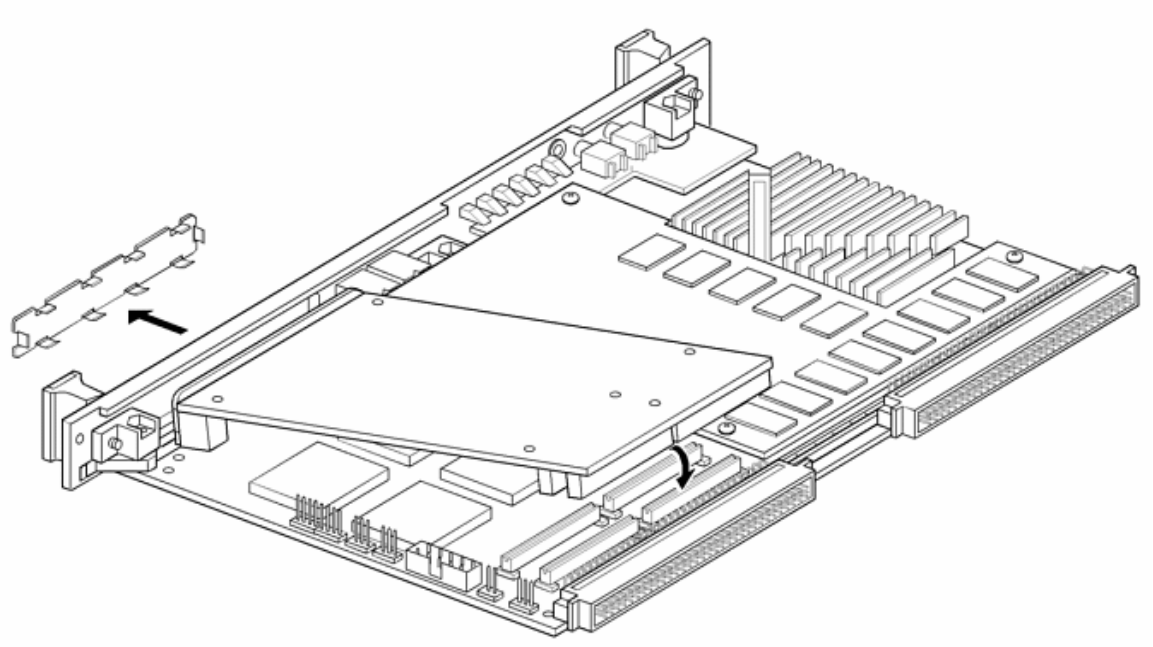
> **Warning!**
>
> Never open the computer without turning off the power supply. Unless internal AC wiring is exposed, leave the power cord plugged in, so as to ground the computer chassis. You can easily get shocked, ruin computer parts or both unless you turn off the power. Even with power switched off, lethal voltages can exist in the equipment.

2. Open the computer and remove the CPU board onto which the VFX-M is to be installed. Identify an empty PMC location (generally there are one or two on a given CPU board).

   The VFX-M uses the 5V signaling protocol, so the registration hole on the VFX-M must match the corresponding index pin on the CPU board.

3. In the interest of allowing air flow, and if you have a choice, try to install the VFX-M in the location which allows the best airflow through card cage.

Figure 2-1 Installation of the VFX-M into a Motorola MVME2604



4. Wear a grounded wrist strap. Touch a metal part of the computer chassis, remove the graphics board from its anti static bag, and immediately slide it into the slot.

Caution

The static electricity that your body builds up normally can seriously damage the integrated circuits on the graphics board. You should first touch the metal part of the chassis, which will short circuit the static charge on your body to ground. It is preferable to wear a grounded wrist strap whenever handling computer boards.

Handle the graphics board only by its edges. Oils from your hand can break down the metal used in the circuit board.

5. Remove the PMC blanking plate from the computer's front panel, and after ensuring that the board is seated correctly, install the mounting screws (two near the front and two near the PMC connectors).

6. Close the computer and plug the VFX-M breakout cable into the VFX-M's front panel. Be sure to snug the thumbscrews down, as the connector may otherwise work loose and cause unreliable operation.

   Connect the VFX-M breakout cable to the video cable for the monitor. The connectors on the VFX-M breakout cable are host side, so you plug a VGA monitor cable into the breakout cable as if it were a connector on the computer's back panel. Make sure that the 75 ohm switch on the monitor is turned on.

> **Note**
>
> The VFX-M can supply 3 Wire (RGB with sync on green, BNC connectors) or 5 Wire Video (RGBHS, VGA connector). Rastergraf software defaults to 5 Wire Video (NO sync on green).
>
> Be aware that if you connect a VFX-M that has video parameters set up for sync on green to a VGA compatible monitor you will get a green background on the display.

2.3.4 Changing the (only) VFX-M Configuration Jumper

The VFX-M is really a "Plug and Pray" device. Its operation is dependent on the software, since there is but one jumper to worry about. The jumper sets the VFX-M to appear in the VGA PCI device sub-class. If the jumper is removed, then the VFX-M appears in the "Other Display Controller" PCI device sub-class. Refer to ***Figure 2-3*** for the location of JP401. The default is to ***install*** the jumper.

Figure 2-2 VFX-M Side 1 Major Parts Locations

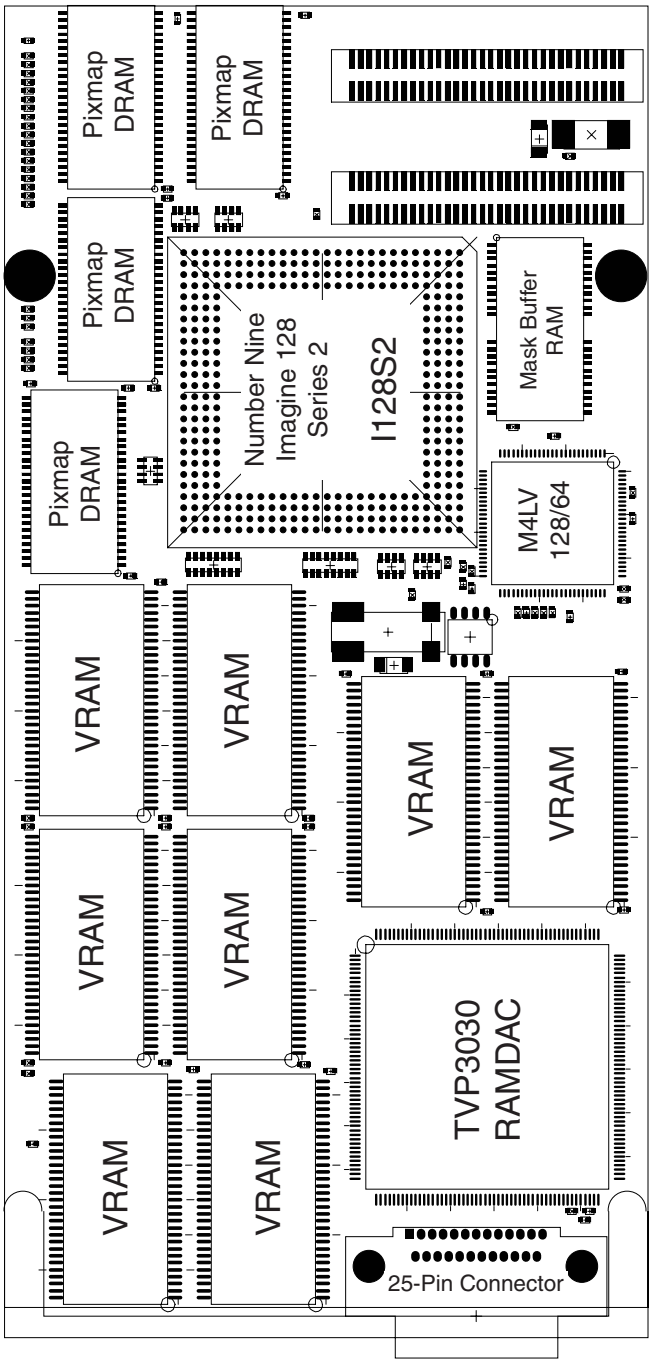
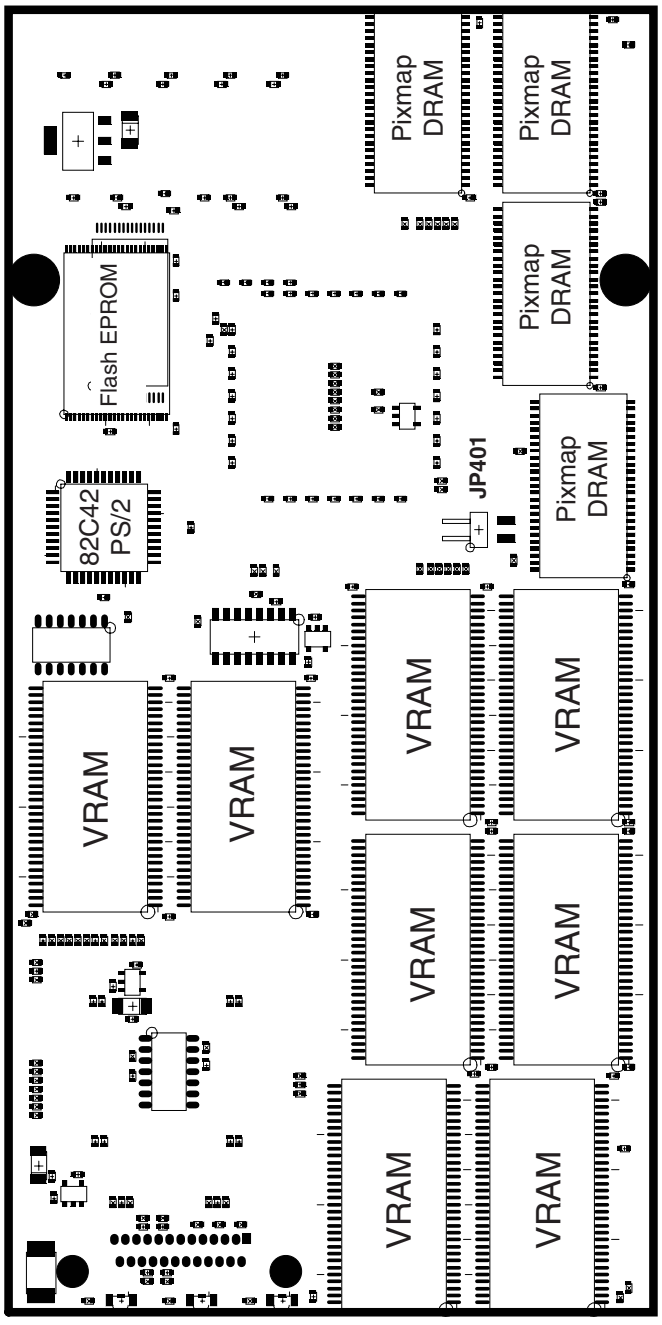


Figure 2-3 VFX-M Side 2 Major Parts Locations



2.4 Checking your Display

Turn on the power and check your monitor's display.

If you are using a PC and the VFX-M is to be the system display board, the system BIOS may find the VFX-M, run its BIOS, and initialize the display.

If you have another VGA type controller in the system, the BIOS will most likely not use the VFX-M for display. If this happens, don't worry.

If you are not running a PC, only after you boot your computer and the graphics board software has been run will you see anything. In the case of PX Windows, your monitor should display a uniform stippled raster and a cross-hair cursor, which is controlled by the mouse. For GLP, demo programs are provided that may be run to put test patterns on the screen.

Once you have a picture on the screen, you may need to adjust the width, height, brightness, contrast, and hold controls on your monitor to get a good, centered image. If these controls don't adjust the image properly, the parameters used to set the graphics timing registers might be wrong.

If you have any trouble with any part of the installation call Rastergraf for assistance, or refer to Chapter 5.

Otherwise, proceed to the instructions supplied in your software manual.

2.5 VFX-M Connections

There is just one connector on the front panel of the VFX-M. It is a 25 pin Cannon MDSM Micro D-sub. It brings all the RGB analog video, Horizontal and Vertical Syncs, and DDC monitor control lines.

A custom made breakout cable, the MVK-1/3, available from Rastergraf, enables standard VGA monitors to be connected. The MDSM end plugs into the VFX-M and is retained with jackscrews. The VGA end duplicates the VGA **board side** connector.

The following sections detail the applicable pinout information.

Breakout Cable Connector Name	**Section**	**Connector**	**Description**
VGA	2.5.1	15-pin D-Sub	VGA
--	2.5.2	25-pin MDSM	Front Panel Connector

2.5.1 Breakout Cable VGA Video Connector

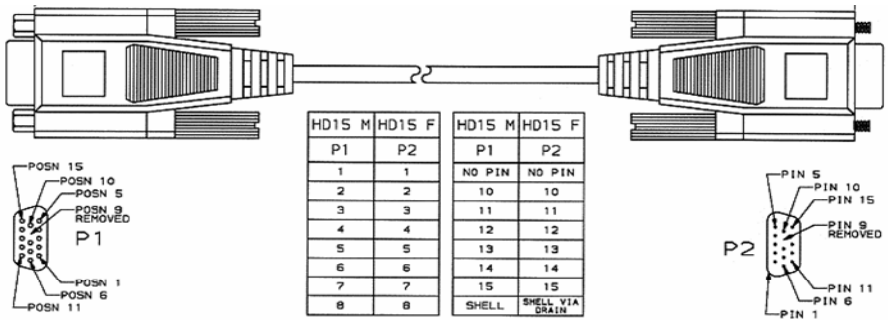
The VFX-M front panel connector supplies analog video to a standard VGA ***computer side*** connector via the Rastergraf MVK-1/3 25-pin Micro-D-Sub breakout cable. The RGB video outputs are driven by the TVP3030 RAMDAC, which is capable of driving terminated cable (75 ohms) to standard RS-330/IRE levels. Cable length should be limited to 50 feet unless you use low loss RG-59.

See the* Note *in Section 2.2.3 concerning composite sync on green and RGBHS video out modes. If you have problems, please contact Rastergraf for assistance.

Table 2-2 VFX-M Breakout Cable VGA Connector Pinout

VGA Pin Number	Description
1	Red
2	Green
3	Blue
4	not used
5	DDC Ground
6	Red Ground
7	Green Ground
8	Blue Ground
9	Fused +5 Volts, .25A max
10	Sync Ground
11	not used
12	DDCDA
13	HSYNC
14	VSYNC
15	DDCCK

Figure 2-4 Typical VGA Extension Cable



2.5.2 VFX-M Front Panel Connector

As mentioned before, the VFX-M uses a 25-pin ITT Cannon MDSM (MDSM-25PE-Z10) connector for the video connections. It is necessary to build a breakout cable to make connections to standard devices. Rastergraf can supply the cable (MVK-1/3) or you can build it yourself.

You can get a 3 foot pigtail from ITT Cannon which has the MDSM connector and a shielded twisted pair cable already made up. All you have to do is wire the other end. The part number is CA111972-12.

Note: The pin list below shows the ITT Cannon pin numbers.

Table 2-3 VFX-M Connector Pinout (sorted by Function)

MDSM Pin Number	Description
1	Blue
2	ground
3	Green
4	ground
5	Red
6	ground
7	not used
8	ground
9	reserved – do not connect
10	ground
11	reserved – do not connect
12	ground
13	Horizontal Sync
14	ground
15	DDCCK
16	ground
17	DDCDA
18	ground
19	reserved – do not connect
20	ground
21	reserved – do not connect
22	ground
23	reserved – do not connect
24	ground
25	Vertical Sync

2.5.5 VFX-M Connections to the PMC Bus

J11			
1	TCKH	n/c (-12V)	2
3	GND	INTAL	4
5	n/c (INTBL)	n/c (INTCL)	6
7	BUSMODE1L	+5V	8
9	n/c (INTDL)	PCI-RSVD	10
11	GND	PCI-RSVD	12
13	PCICLK	GND	14
15	GND	PMCGNTL	16
17	PMCREQL	+5V	18
19	Vio	AD31H	20
21	AD28H	AD27H	22
23	AD25H	GND	24
25	GND	C/BE3L	26
27	AD22H	AD21H	28
29	AD19H	+5V	30
31	Vio	AD17H	32
33	FRAMEL	GND	34
35	GND	IRDYL	36
37	DEVSELL	+5V	38
39	GND	LOCKL	40
41	n/c (SDONL)	n/c (SBOL)	42
43	PAR	GND	44
45	Vio	AD15H	46
47	AD12H	AD11H	48
49	AD09H	+5V	50
51	GND	C/BE0L	52
53	AD06H	AD05	54
55	AD04H	GND	56
57	Vio	AD03H	58
59	AD02H	AD01H	60
61	AD00H	+5V	62
63	GND	n/c (RQ64L)	64

J12			
1	+12V	TRSTL	2
3	TMSH	TDOH	4
5	TDIH	GND	6
7	GND	PCI-RSVD	8
9	PCI-RSVD	PCI-RSVD	10
11	BUSMODE2L	byp (+3.3V)	12
13	RSTL	BUSMODE3L	14
15	byp (+3.3V)	BUSMODE4L	16
17	PCI-RSVD	GND	18
19	AD30H	AD29H	20
21	GND	AD26H	22
23	AD24H	byp (+3.3V)	24
25	IDSEL1	AD23H	26
27	byp (+3.3V)	AD20H	28
29	AD18H	GND	30
31	AD16H	C/BE2L	32
33	GND	PMC-RSVD	34
35	TRDYL	byp (+3.3V)	36
37	GND	STOPL	38
39	PERRL	GND	40
41	byp (+3.3V)	SERRL	42
43	C/BE1L	GND	44
45	AD14	AD13H	46
47	GND	AD10H	48
49	AD08H	byp (+3.3V)	50
51	AD07H	PMC-RSVD	52
53	byp (+3.3V)	PMC-RSVD	54
55	PMC-RSVD	GND	56
57	PMC-RSVD	PMC-RSVD	58
59	GND	PMC-RSVD	60
61	n/c (AK64L)	byp (+3.3V)	62
63	GND	PMC-RSVD	64

Note: **byp** means the pin is connected to a bypass capacitor on the VFX-M, but is otherwise not used

Chapter 3
Software Summary

3.1 Introduction

This chapter provides an overview of Rastergraf's software offerings. Rastergraf also has Software Product Descriptions and complete Technical Manual sets for its Software products. Software is shipped by FTP and on CD-ROM media.

Since the VFX-M does not have an on-board CPU, all software functions are executed by the host CPU. In order to optimize system performance, you should take into account the CPU overhead and additional memory requirements imposed by the software. Please contact Rastergraf if you have any questions regarding this or need assistance in optimizing your applications.

Rastergraf provides software for the VFX-M including:

PX Windows	X11R6 X Windows Server
GLP	Graphics Library Package with Direct OpenGL Library (doesn't use X)
NT Drivers	Windows NT 4.0 Native Driver set
Tru64 Driver	A device driver that allows the VFX-M to operate in the Tru64 UNIX X Windows environment

The following table summarizes the software both planned and currently available for the VFX-M. Contact Rastergraf if your choice is not shown.

3.2 Software Availability by Platform and OS

Table 3-1 Rastergraf Software and Operating Systems Support

Operating System	Current OS Version	CPU Type	Supported Software
LynxOS	3.0	PowerPC	GLP
LynxOS	3.0	PowerPC	PX Windows
Tru64 UNIX (AKA Digital Unix)	4.0	Alpha	Driver for Tru64 X Windows Server
Solaris*	2.6	SPARC	PX Windows
Windows NT*	4.0	Alpha	Native Drivers, VGA BIOS
Windows NT	4.0	x86	Native Drivers, VGA BIOS
VxWorks	Tornado	PowerPC	GLP
VxWorks*	Tornado	PowerPC	PX Windows

* contact Rastergraf for availability

3.3 Write Posting

Most CPU designs include pipelining and write posting. The CPU, which is much faster than the host bus interface, is allowed to store (or post) a write operation to the CPU board's Host bus controller. The controller takes care of the write within the timing requirements of the Host bus. Pipelining is a procedure whereby the CPU can process more than one instruction at a time. As a result, instructions are not necessarily completed in the order that they were started.

For example, if you wanted to first change a control register in I128S2 chip and then write to its associated frame buffer, you are not guaranteed that the writing order is preserved. This could result in an incorrect operation. The way to get around this is to insert memory barrier instructions between these write operations. Rastergraf's software is already tailored to correct this problem.

3.4 PX Windows Server

X Windows is a machine independent network based windowing system. It divides graphics functions into two parts:

1) The server, which controls the hardware dependent functions such as the mouse, keyboard or trackball, and graphics display; and

2) The client(s), which is (are) the actual programs which the user wants to interact with. This might include a terminal emulator, desktop publishing program, or an image processing package. The client application is usually linked with the standard Xlib library which manages the actual communications between clients and the server.

Rastergraf supplies the hardware specific parts of the X Window System, in other words, the server. Most operating systems come supplied with a local Xlib and a standard client package including the Motif window manager. Contact your OS vendor for specifics on what they supply.

Under certain circumstances and for particular operating systems, Rastergraf can supply an extended version of PX Windows which includes a client side package (including Motif). Please contact Rastergraf for availability.

Rastergraf's PX Windows Server is a Motif client compatible X Windows X11R6 board based server.

3.5 Graphics Library Package

The Graphics Library Package (GLP), comprises a significant value-added component for the Rastergraf display controllers. It is intended for the user who wishes to interface an application directly to the board without going through a standard windowing system like Windows NT or the X Window System. The GLP provides a high-level, powerful, flexible yet low-overhead interface to the applications programmer. A full set of graphics operations can be performed without contending with all the hardware details, yet direct access to board registers is available for those applications which require it.

The GLP is a collection of libraries that provide different levels of API (applications programming interface) for the user. These libraries are compatible with BSD and System V Unix and many real-time operating

systems, and provide functions for configuring the Rastergraf display controller in an OS-independent way.

A sophisticated set of rendering functions is provided that allows the user to use the same extensive set of drawing methods to create an image, whether on the visible display or in Pixmap memory, just by changing the "drawable" on which the application routine operates. Drawing methods are implemented in the way that gives the best performance. Sometimes this uses the I128S2 graphics processor, sometimes rendering is done by directly altering pixels in the drawable. Support for font characters (software-defined patterns drawn in the graphics memory) is provided with Rastergraf's ***TI Font Set,*** a font package derived from the Hershey bit-mapped fonts, and with ***FreeType,*** a public domain package which allows you to use TrueType fonts.

Initialization functions, demo programs and utilities are included with the GLP. Most programs are supplied in source and executable and are written in C. A list of the Graphics Library Functions is available upon request.

OpenGL Support

Although it is a Silicon Graphics OpenGL Level II source licensee, Rastergraf has elected to base most of its OpenGL compatible extension to the GLP on ***MesaGL***, a freeware clone of OpenGL. The resulting package will successfully run the SGI OpenGL compliance suite.

This approach was taken because MesaGL offered a cleaner code base for providing a close interface between OpenGL and the VFX-M hardware. And, unlike other implementations, no windowing system (e.g. X Windows) is required to use it. Rastergraf has also added font support.

All upper level OpenGL operations are directed through the VFX-M hardware specific layer, which is a collection of routines optimized for different kinds of span drawing functions.

3.6 NT Native Drivers

The NT Native Drivers are the Windows NT 4.0 minport and display drivers and a VGA BIOS. They are derived from code received from a third party. They allow the VFX-M to function seamlessly as the PC console and graphics display in any x86 system. As currently released, they are not 64 bit clean and will not run in an Alpha system.

3.7 Tru64 UNIX Driver

The Tru64 Driver Kit allows the VFX-M to be seamlessly integrated into the Compaq Tru64 UNIX X Windows WorkStation (WS) environment.

The driver enables the Tru64 X Server to access the VFX-M's color map, display controller registers, and frame buffer. Note that at the time of this writing, the driver relies on the X Server's CFB (Color Frame Buffer) software to perform all drawing operations. It is, therefore, not a hardware-optimized server, and does not use any I128S2 accelerated graphics functions.

When you have a dual-processor 21264 Alpha, this is not a deficiency. However, depending on customer needs, for those that don't, some acceleration may be added in the future. Please contact Rastergraf for more information.

Chapter 4
Programming On-board Devices and Memories

4.1 Introduction

This chapter covers the special programming features of the individual devices used on the VFX-M. It is intended to supply information unique to the board or to the application of a particular chip. Section 1.3 provides a list of appropriate publications that include manufacturer's data sheets and manuals.

Rastergraf offers a variety of software to support the VFX-M in both Unix and real-time environments. These offerings are covered in detail in Chapter 3. Software includes:

Demo Programs	To make the software easy to use
PX Windows	X11R6 X Windows Server
GLP	Graphics Library Package with Direct OpenGL Library (doesn't use X)
NT Drivers	Windows NT 4.0 Native Driver set
Tru64 Driver	A device driver that allows the VFX-M to operate in the Tru64 UNIX X Windows environment

Note

Please read these sections **before** starting on this chapter:

Section 1.2	Functional description of the VFX-M board.
Chapter 2	Installation
Chapter 3	Summary of software support from Rastergraf.

This chapter includes the following other sections:

4.2 Imagine 128 Series 2 (I128S2) Graphics Accelerator
4.3 VFX-M Auxiliary Registers
4.4 TVP3030 RAMDAC
4.5 Video Timing Parameters
4.6 VFX-M Interrupts
4.7 Flash EEPROM
4.8 Serial EEPROM

Because the VFX-M is mostly an assembly of "black box" parts, there isn't a lot of external logic that has to be documented. Thus, the following sections don't actually provide much programming information, as the chip documentation and GLP source code cover that pretty well. The sections summarize the devices and include some "hints and kinks".

The following sections assume that you have read Section I.2 and have some knowledge of the PCI bus. For detailed information concerning operation of the PCI bus, please refer to the Section I.3, Additional References.

Time Saving Note

One thing that isn't obvious from the block diagram is that the ***TVP3030 RAMDAC*** (Section 4.4) and the ***VFX-M Auxiliary Control Register*** (Section 4.3) share the 16 register block in the I128S2 that is allocated to the RAMDAC. This is explained in Section 4.2.10.

4.2 Imagine 128 Series 2 (I128S2) Functional Unit

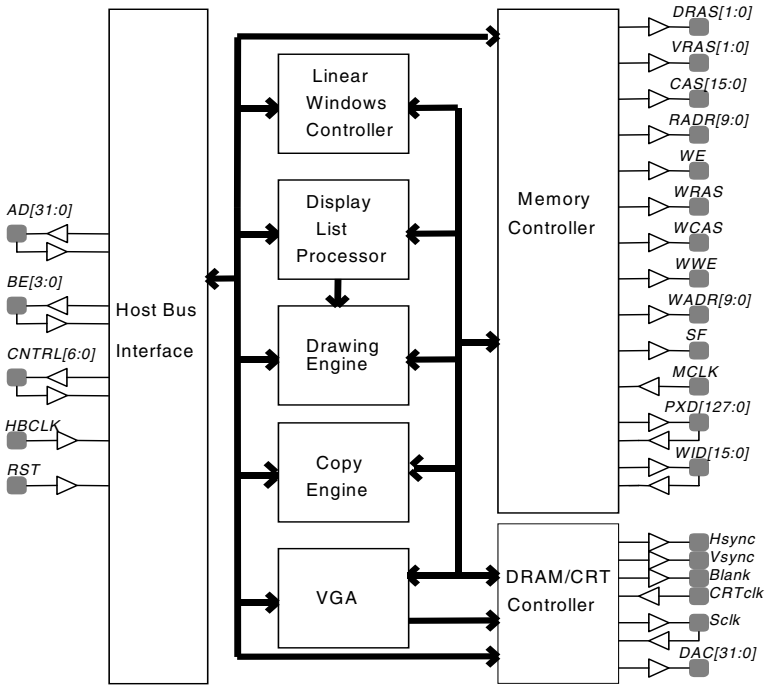
> **Note**
>
> The ***I128S2 Technical Manual*** is available from Rastergraf under NDA..

Looking at the Block Diagram, there are eight components of the I128S2:

- PCI Bus Interface
- Memory Controller
- CRT Controller
- VGA Core
- Aperture Controller
- Display List Processor
- Drawing Engine
- Copy Engine

Of these, the PCI Bus Interface, Memory and CRT controllers, and VGA Core are covered in this Section. The Aperture Controller, Display List Processor, Drawing Engine, and Copy Engine are I128S2 internal units and are covered in the ***I128S2 Technical Manual***.

Figure 4-1 I128S2 Block Diagram



4.2.1 PCI Bus Interface

Although the actual PC boards are radically different, the standard PCI bus board and the VFX-M are virtually identical when it comes to the electrical side of things. The Number Nine I128S2 serves not only as the graphics controller but also as the PCI bus interface.

The VFX-M uses the I128S2 to provide the PCI 2.1 32-bit 33 MHz compliant bus interface. PCI signals connect to the I128S2 only. The placement and routing is done to the PCI specifications, keeping the trace lengths to 1.5" for bus signals and 2.5" for the clock.

In addition to providing the actual 32-bit data path between PCI bus and the I128S2 internal registers and 128-bit wide memory path, the I128S2 performs the PCI/local address mapping and decoding. It has on-chip FIFOs for buffering data.

The I128S2 has decodes for: PCI Configuration Registers, Copy and Drawing Engine Registers, one XY and two Linear Memory Windows for accessing VRAM and DRAM, Flash PROM Window, I/O Register Window, and a VGA Core register set. Except for the PCI Configuration Registers, which have a fixed size and address, each decode has a Base Address Register (BAR) associated with it.

The I128S2 also provides mapping for the Mask Buffer DRAM and the RAMDAC. Since the VFX-M has a configuration EEPROM and three diagnostic LEDs, the RAMDAC address space is partitioned into subsections to allow access to these additional devices without having to add another PCI interface. A Lattice M4LV128/64 PLD decodes the address space and provides chip selects for the devices. It also is used for miscellaneous functions such as video blanking and sync delay and clock drivers.

4.2.2 Video RAM (VRAM)

The display memory chips are expressly designed for high speed graphics applications. These devices are called Video RAMs (VRAMs).

They are like ordinary DRAMs, but they also contain an internal 256 x 16 line buffer. The VRAMs have a mode control input (DT/OE), which is used to trigger a data transfer to the line buffer. When DT/OE is active as RAS is asserted, a data transfer cycle occurs. The row address selects a line of data, and the column address selects the starting position within that line. The data are then shifted out by a serial clock, 16 bits/clock appearing at the outputs.

The VRAM output shift registers supply 128 bits of pixel data every shift clock to the TVP3030. Depending on the pixel size, this corresponds to sixteen 8-bit pixels, eight 16-bit pixels, or four 32-bit pixels.

The data transfer operation has to be repeated only two or three times, at most, during a raster line time. The VRAM is available for random access operations at all other times. There is a small additional overhead time for memory refresh, which occurs about once every 15 us. VRAM availability for external access is about 95% as compared to about 35% for DRAM. The VFX-M uses TI TMS55161 256K x 16 2-port EDO VRAM.

Write-per-bit Registers

VRAM has a write-per-bit feature that allows bit planes to be selectively write enabled. This feature allows the I128S2 to perform write operations instead of read-modify-write operations, which can be a significant performance enhancement. When updated, the I128S2 write-per-bit register contents are automatically stored in the VRAM using the persistent write-per-bit function. The write-per-bit register has no effect on the Pixmap (DRAM) Memory.

VRAM Color Register and Block Fill Special Function

The I128S2 can use the VRAM block write and color register special functions. The color register is used in conjunction with the VRAM block fill mode to enable up to 4 adjacent locations in the VRAM to be written in one cycle. In this way, one can quickly replicate 1-D and 2-D patterns in memory at up to 16 times the single pixel rate. Using block write, up to 64 (16 byte data bus * 4 locations/block) 8-bit pixels can be written in each 40 ns page mode cycle, resulting in a 1600 Mpixel/sec FILL time.

Display Memory Size

The pixel size programmable to 8, 16, or 32 bpp. Although the RAMDAC supports packed 24-bit mode, the I128S2 does not. The VRAM on the VFX-M can be either 4 MB (4,194,304 bytes) or 8 MB (8,388,608 bytes). You can calculate the possible display formats based on these values.

Note that you can render into VRAM that is not being used in the active display, and by changing the starting address register in the I128S2, pan to it so it is visible or BitBLT the Pixmap data to a static display window.

4.2.3 I128S2 Pixmap Memory (DRAM)

The I128S2 Pixmap Memory is independent of the VRAM. It shares a common address space with the display memory and can thus be rendered to (***but you can't use VRAM special functions***) or used for Pixmap display data. The memory size is 64 MB (67,108,864 bytes) of no-wait state EDO DRAM.

The Pixmap Memory is divided into two 32 MB sections. A control bit in the VFX-M Auxiliary Control Register is used to select between the two banks. This means that the I128S2 cannot access the unselected half of memory.

4.2.4 I128S2 Mask/WID Buffer Memory

In addition, the I128S2 has a 2 MB Mask/WID Buffer DRAM. The main purpose of the memory is to provide arbitrary clipping or WID masking for all display memory writes. The mask buffer address and data bus lines are separate from the display/private memory address and data busses, and are shared with the RAMDAC and other control logic.

4.2.5 Memory Controller

The I128S2 shares access to the Display and Pixmap memories with the PCI bus by means of the I128S2's memory controller. When accessed by the PCI bus, the display and system RAM are byte addressable.

The I128S2's hardware byte-swapper can be used to streamline host bus accesses. This can be useful if you are using a PowerPC CPU to pass data to graphics memory, as the PowerPC is a big endian chip and the PCI bus and I128S2 are little endian. You can save a CPU swap operation. Depending on the amount of data transferred between the CPU and the graphics memory, the swapper can give between 5 and 15% performance boost. The I128S2's PCI Memory Windows can be programmed to support swapped or non-swapped memory access.

The I128S2 operates on memory in 1, 2, 4, 8, or 16 byte segments. It also supports page-mode read and write memory accesses for maximum memory performance. For graphics memory, VRAM color register, block fill and write-per-bit functions are supported. The I128S2 derives its memory timing from a clock which is **independent** of the video clock. The I128S2 has internal synchronizers which take care of VRAM memory accesses (CPU clock synchronous) and VRAM shift, load, and blank

functions (video clock synchronous). The I128S2 has inputs for the VRAM shift and load clocks so that it can keep track of blanking.

There are three secondary buses on the I128S2: the 128-bit **PIX** bus, the 32-bit **DD** bus, and the 16-bit **MBD** bus.

PIX Bus

The 128-bit **PIX** memory data bus is connected directly to the Video RAM (VRAM) and pixmap display memory (DRAM). The VFX-M can have a maximum of 8 MB of VRAM display memory and 64 MB of DRAM.

DD Bus

As shown in the Block Diagram, the VRAM output shift registers are ordinarily the source display data and drive the RAMDAC. However, in order to support the display features of VGA, display data has to be passed through the I128S2's VGA core first: pixel data is read a raster line at a time from the VRAM (over the PIX bus) and piped through an internal FIFO to the core. The low 8 bits of the **DD** bus provide the VGA pixel data from the core to the RAMDAC's special VGA port. This is sufficient for 640 x 480 displays. The TVP3030 PLLs come up in a default VGA mode, so they don't need to be set up. The DD bus is also utilized in a design which has DRAM for display memory. The VFX-M doesn't make use of this feature.

MBD Bus

The **MBD** bus serves as a separate "private" data bus for the RAMDAC, VFX-M control register, and Mask Buffer RAM, and there are two address spaces for this bus: one for the Mask Buffer RAM, the other for the RAMDAC. The M4LV-128/64 PLD controls access to the RAMDAC address space, and allows it to be shared among the RAMDAC and VFX-M control register.

4.2.6 I128S2 VGA Support

The VGA core is only used to provide basic PC compatibility, and is a device unto itself, independent of the primary CRT Controller section. From an external standpoint, it shares the memory and CRT control lines with the CRT Controller and Memory Controller. The VGA Core is described at some length in the I128S2 Technical Manual.

4.2.7 I128S2 Clocks

The I128S2 has five clocks: DECLK, MCLK, VCLK, LDCLK, and SCLK

DECLK is the drawing engine clock. It is derived from the CY2292 clock synthesizer. On power up, it is set 40 MHz. Once FS1 (see Section 4.4) is set, the TVP3030's PLLs are enabled and DECLK is set to 50 MHz.

VCLK is the clock used by the I128S2's CRT Controller to generate video timing. **MCLK** is the clock used by the I128S2 to time all local memory accesses. VCLK and MCLK are driven by independent PLL clock synthesizers in the TVP3030 RAMDAC.

SCLK is used to shift data out of the VRAM video data output shift registers. It is derived by gating VCLK with blanking and is therefore active only during the visible part of the display interval.

The MCLK and VCLK frequency source is controlled by Frequency Select bits FS1 and FS0 according to the table shown on the following page. below. FS1 and FS0 are connected to the TVP3030 PLLSEL1 and PLLSEL0, respectively.

FS0 is derived from I128S2's VGA core, Port (write) 0x03C2, bit *d2*. Bit *d3* might be construed as FS1, but it doesn't actually do anything. FS1 comes from the VFX-M Auxiliary Control Register (see Section 4.5).

When the VFX-M powers up, the memory and video clocks default to VGA compatible standard frequencies, such that MCLK is 50.11 MHz and VCLK is 25.057 MHz.

Once the VGA BIOS (or, if in a non-PC environment, the VFX-M graphics software) is executed, the MCLK and VCLK PLLs can be programmed to select higher frequencies in accordance to the desired display format and memory timing. Typically, the memory clock is 100 MHz, while the video clock is 170 MHz.

LDCLK is an auxiliary clock output from the I128S2 and is not used in the VFX-M design.

The following table details how FS1 and FS0 affect the clock frequencies.

Table 4-1 MCLK and VCLK Frequency Selections

FS1	FS0	DECLK	MCLK	VCLK
0	0	40 MHz	50.11 MHz	25.057 MHz
0	1	40 MHz	50.11 MHz	28.636 MHz
1	0	50 MHz	MPLL	VPLL
1	1	50 MHz	MPLL	VPLL

Notes: MPLL and VPLL are the frequencies resulting from parameters programmed into the TVP3030's Memory and Video PLL clock synthesizers.

FS1 is programmed via the VFX-M Auxiliary Control Register.
FS0 is programmed via the I128S2 VGA Core (see previous page)

A consequence of the dual clock nature of the I128S2 is that if you read a register driven by the pixel clock (e.g. VCOUNT), you may get erratic results. You have to read the comparison flag or use interrupts to get correct results. The reason for this is simple: the VCOUNT register can change state in the middle of an I128S2 read cycle. Its operations are totally asynchronous to the I128S2 PCI bus interface clock.

4.2.8 I128S2 Build Options and Power-up Settings

The I128S2 is a "Plug and Pray" device, whose operation depends on the software. Except for the VGA mode option, there are no user jumpers. However, the Technical Manual documents a number of register preloads and functional settings that are read by the I128S2 on power up.

Note: Type = **soft** means that the value can be overridden by software.

Type = **hard** means that the value cannot be changed by software. Please contact Rastergraf if it is necessary to change a value.

Table 4-2 I128S2 Configuration Jumper Settings

CJ	In/Out	Type	Function	Default
00	out	soft	PCIBAR 0 address size	16 MB for video memory
01	in	soft		
02	in	soft	PCIBAR 1 address size	32 MB for pixmap memory
03	in	soft		
04	out	soft	PCIBAR 2 address size	4 MB for mask memory (minimum allowed)
05	out	soft		
06	out	soft	PCIBAR 3 address size	4 MB (minimum allowed)
07	out	soft		
08	out	soft	PCIBAR_ROM address size	128 KB for Flash
09	in	soft		
10	out	soft		
25	in	hard	VRAM density	256K x N
26	out	hard		
27	in	soft	VRAM banks	2 banks
28	out	hard	DRAM density	1M x N (CJ29 = out >> none)
29	in	soft		
30	in	soft	DRAM banks	2 banks
31	out	hard	mask memory density	1M x N (CJ32 = out >> none)
32	in	soft		
33	in	soft	RAS width	4 MCLKs
34	in	soft	interrupt enable	Enabled
36	out	hard	PCI device sub class	(CJ37 = in >> other) (CJ37 = out >> VGA)
37	out	JMP		
38	in	soft	BIOS PROM enable	Enabled
39	in	soft	pixel data bus size	128 bit
40	out	hard	spare	-
41	in	soft	fast back to back	Enabled

CJ	In/Out	Type	Function	Default
42	out	hard	spare	-
43	out	hard	ISA bridge timing	no bridge function
44	in	soft	merge memory requests	Enabled
45	out	hard	spare	-
46	in	soft	linear memory prefetch	Enabled
47	out	hard	spare	-
48	out	hard	spare	-
49	in	soft	EDO/Fast Page	EDO
50	out	soft	VRAM bank transfers	Unique
51	in	soft	RAS to CAS delay	4 MCLKs
52	out	soft	memory refresh	refresh every 768 clocks
53	out	soft		
54	in	hard	VGA type	internal VGA, not bridge
55	out	hard	Subsystem Vendor ID	Rastergraf PCI Vendor ID 0x10F0
56	out	hard		
57	out	hard		
58	out	hard		
59	in	hard		
60	in	hard		
61	in	hard		
62	in	hard		
63	out	hard		
64	out	hard		
65	out	hard		
66	out	hard		
67	in	hard		
68	out	hard		
69	out	hard		
70	out	hard		
71	out	soft	Subsystem ID	Subsystem ID Code
72	out	soft		
73	out	soft		
74	out	soft		
75	out	soft		
76	out	soft	Enable User Vendor ID	Enabled

Note: the subsystem ID on rev 0 boards is “hard” 0x1F, and some “spare” bits are 1.

4.2.9 Page Faults and Autoincrement Registers

When copying data to the host from the auto-incrementing registers (color palettes) one must be careful about page faulting. Before reading the color map, you should lock a memory block and "touch" the variable(s) you are copying to ensure that they are in CPU memory. If you don't, you may get a page fault which would force a retry of the instruction. A **second read** of a location will occur when the instruction is retried, because the entry was already read once when the page fault occurred.

4.2.10 RAMDAC Address Space

The I128S2 has a 16 register space that is nominally allocated to the RAMDAC. As the VFX-M has not only the RAMDAC, but also miscellaneous control bits and LEDs to deal with, the 16 register space has been partitioned to accommodate these requirements.

Table 4-3 I128S2 RAMDAC Address Space

FCN	DAC Register Address	Register Mnemonic	RAMDAC Address Space Utilization
0	0x0 - 0x5	-	TVP3030 DAC access
	0x6	VFX_ACR	VFX Auxiliary Control Register
	0x7	-	TVP3030 DAC access
	0x8	VFX_ASR	VFX Auxiliary Status Register
	0x9 - 0xF	-	TVP3030 DAC access
1	0x0	reserved	reserved
	0x1	reserved	reserved
	0x2 - 0x5	-	reserved
	0x6	VFX_ACR	VFX Auxiliary Control Register
	0x7	-	reserved
	0x8	VFX_ASR	VFX Auxiliary Status Register
	0x9	-	reserved
	0xA	VFX_RAL	Low 8 bits of the Horizontal Line Counter
	0xB	VFX_RAH	High 4 bits of the Horizontal Line Counter
	0xC - 0xF	-	reserved

See Section 4.3 for specific register bit definitions.

4.3 VFX-M Auxiliary Registers

Although most functions on the VFX-M are self-contained, it is necessary to maintain a few extra control bits and supplementary features. Since there is no other convenient way to support these functions, the 16 register RAMDAC address space is used. Section 4.2.10 details the address partitioning. This section covers the actual control bits.

Table 4-4 VFX_ACR Register Bit Assignments

Bit	Mnemonic	Read/Write	Function
0	REDLED	yes	Turn on the Red LED. Can be used as a diagnostic indicator.
1	AMBLED	yes	Turn on the Amber LED Can be used as a diagnostic indicator.
2	GRNLED	yes	Turn on the Green LED Can be used as a diagnostic indicator.
3	BANKSELH	yes	Select the High 32 MB of DRAM. The I128S2 can only access the top or bottom half of the DRAM at any time. Drives A10 pin on the DRAMs.
4	FS1	yes	Pixel Clock Select Drives the FS1 pin on the RAMDAC. The I128S2 VCSEL pin controls the FS0 pin on the RAMDAC. FS1 and FS0 select the DECLK, VCLK, and MCLK. FS1 is also called PLLSEL1.
5	reserved	yes	Reserved – write with 0
6	reserved	yes	Reserved – write with 0
7	reserved	yes	Reserved – write with 0

Table 4-5 VFX_ASR Register Bit Assignments

Bit	Mnemonic	Read/Write	Function
0	reserved	Read-only	reserved
1	reserved	Read-only	reserved
2	BLANKL	Read-only	High when Display is Active. Use with VFX_RAL and VFX_RAH to determine when it is OK to access the TVP3030 RAMDAC.
[3:7]	FIRMCODE[0:4]	Read-only	PLD Firmware Code 5-bit code indicates the firmware revision level. Currently reads [00001]. If FIRMCODE reads [00000] the BIOS PROM will not work.

Table 4-6 VFX_RAL Register Bit Assignments

Bit	Mnemonic	Read/Write	Function
[0:7]	VFX_RAL[0:7]	Read-only	Low 8 bits of the Horizontal Line Counter Use with BLANKL to determine when it is OK to access the TVP3030 RAMDAC. Reset to 0 at the onset of Vertical Sync.

Table 4-7 VFX_RAH Register Bit Assignments

Bit	Mnemonic	Read/Write	Function
[0:3]	VFX_RAH[0:3]	Read-only	High 4 bits of the Horizontal Line Counter Use with BLANKL to determine when it is OK to access the TVP3030 RAMDAC. Reset to 0 at the onset of Vertical Sync.

4.4 TVP3030 RAMDAC

The following information is derived from the Texas Instruments TVP3030 data sheet. You can obtain the complete data sheet from the TI web page: http://www.ti.com/sc/docs/folders/analog/tvp3030.html

The TVP3030 is an advanced Random Access Memory Digital to Analog Converter (RAMDAC). The TVP3030 has a 128-bit wide video input port, enabling 24-bpp displays at resolutions up to 1600 x 1280 at a 76-Hz refresh rate. 24-bpp graphics at 1280 x 1024 resolution may be implemented at even higher refresh rates. A 128-bit wide pixel bus provides a 4:1 24 bpp mode (128-bit bus width for overlay and RGB). The byte router function allows pseudo-color or monochrome image data to be taken from the red, green, or blue color channels. This enables high performance 24-bpp architectures organized as red, green, and blue memory banks to provide 8-bpp modes as well.

The TVP3030 supports many pixel formats. Data can be split into 4 or 8 bit planes for pseudo-color mode or split into 12-, 16- or 24-bit true-color and direct-color modes. For the 24-bit direct color modes, an 8-bit overlay plane is available. The 16-bit direct- and true-color modes can be configured to IBM XGA [565], TARGA [5551], or [664] as another existing format. An additional 12-bit mode [4444] is supported with 4 bits for each color and overlay. All color modes support selection of little or big endian data format for the pixel bus. The TVP3030 is software compatible with the TVP3026 and Bt476/8 color palettes.

Note that while the TVP3030 also supports 24 bpp packed modes, the I128S2's accelerated functions do not. Nevertheless, Rastergraf's GLP software will operate correctly, but uses the I128S2 only in "dumb framebuffer" mode.

Two fully programmable PLLs for pixel clock and memory clock functions are provided for dramatic improvements in graphics system cost and integration. A third loop clock PLL is incorporated making pixel data latch timing much simpler than with other existing color palettes. In addition, an external digital clock input is provided for VGA modes. The reference clock output is driven by the loop clock PLL and provides a timing reference to the graphics accelerator. The shift clock output may be used directly as the VRAM shift clock.

The TVP3030 also integrates a complete, IBM XGA-compatible hardware cursor on chip, making significant graphics performance enhancements possible. Additionally, color-keyed switching is provided, giving the user

an efficient means of combining graphic overlays and direct-color images on-screen.

The TVP3030 has three 256-by-8 color lookup tables with triple 8-bit video digital-to-analog converters (DACs) capable of directly driving a doubly terminated 75-Ω line. The lookup tables are designed with a dual-ported RAM architecture that enables ultra-high speed operation. The device features a separate VGA bus which supports the integrated VGA modes in graphics accelerator applications, allowing efficient support for VGA graphics and text modes. The separate bus is also useful for accepting data from the feature connector of most VGA supported personal computers, without the need for external data multiplexing.

The TVP3030 is connected to the serial port of VRAM devices without external buffering. It also supports the split shift-register transfer operation, which is common to many industry standard VRAM devices. To aid in manufacturing test and field diagnosis, several highly integrated test functions have been designed to enable simplified testing of the palette and the entire graphics subsystem.

Feature Summary

- Supports Resolutions up to 1600 × 1280 @ 86-Hz Refresh Rate
- Color Depths of 4, 8, 16, 24 and 32 bpp at Maximum Resolution
- 128-Bit-Wide Pixel Bus
- Versatile Direct-Color Modes:
  - 24-bpp with 8-Bit Overlay (O, R, G, B)
  - 16-bpp (5, 6, 5) XGA and 16-bpp (6, 6, 4) Configurations
  - 15-bpp With 1 Bit Overlay (1, 5, 5, 5) TARGA Configuration
  - 12-bpp With 4 Bit Overlay (4, 4, 4, 4)
- True-Color Gamma Correction
- Programmable Frequency Synthesis PLLs for Dot and Memory Clocks
- Loop Clock PLL Compensates for System Delays
- 64 × 64 × 2 Bit-mapped Cursor (XGA and X-Windows Compatible)
- Byte Router Allows Use of R, G, or B Direct-Color Channels Individually
- Direct Interfacing to Video RAM
- Supports Overscan for Creation of Custom Screen Borders
- Color-Keyed Switching of Direct Color and True Color or Overlay
- Triple 8-Bit D/A Converters
- Analog Output Comparators for Monitor Detection
- RS-343A Compatible Outputs
- Direct VGA Pass-Through Capability
- Palette Page Register
- Horizontal Zooming Capability

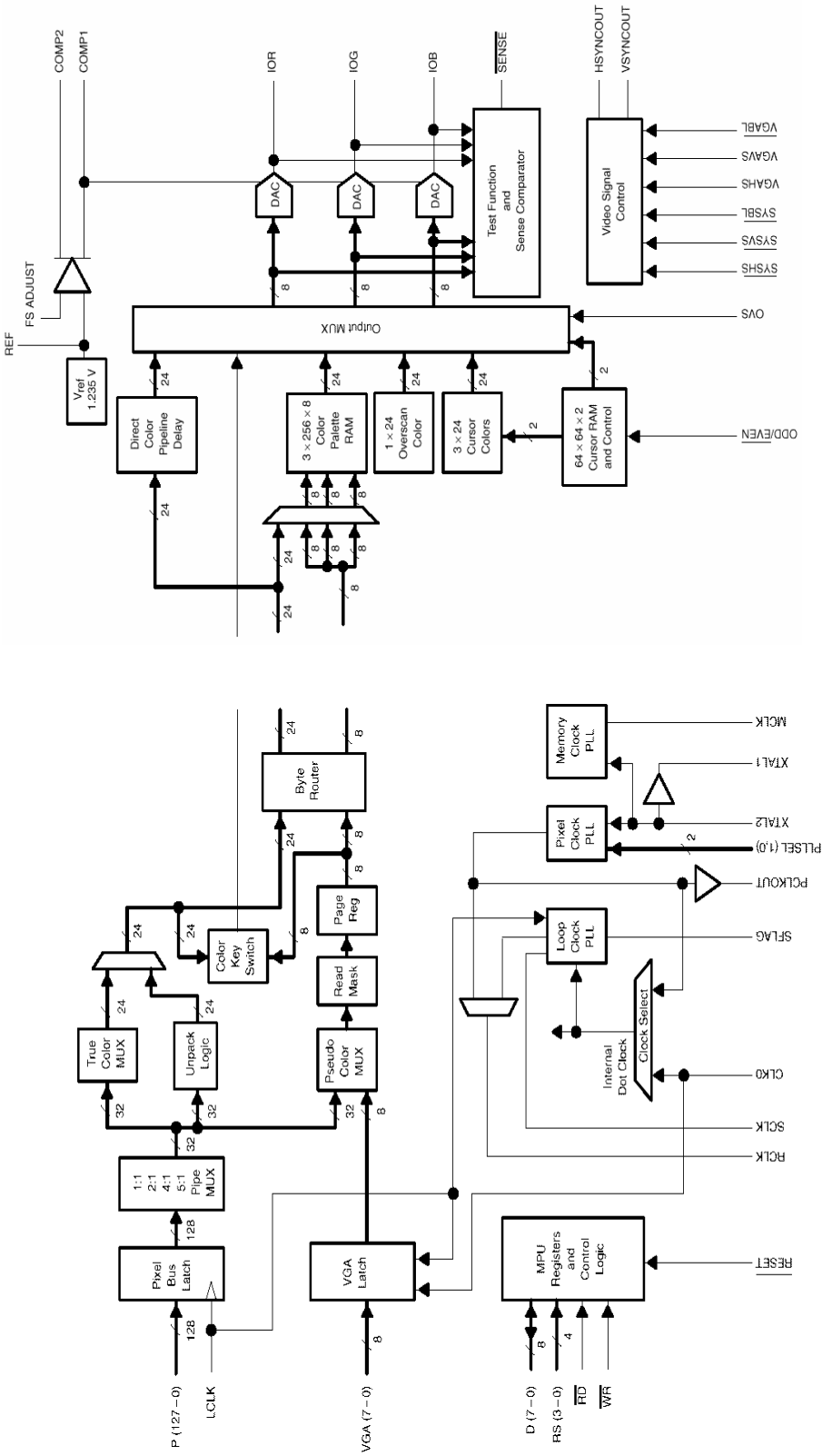


Figure 4-2 TVP3030 Block Diagram

4.5 Video Timing Parameters

The I128S2 must be programmed to generate the proper video timing for the hardware configuration and display format. Rastergraf's Graphics Library Package (GLP) accepts display format (e.g. 1600 x 1280, 32 bpp) and refresh requirements (e.g. 67 Hz vertical refresh) as parameters to a function call. The software then provides (and loads) a best fit timing profile for the I128S2 graphics chip.

Similar display format information is provided in a configuration file for Rastergraf's PX Windows server.

Does your Display have a Green Cast to it?

By default, the VFX-M supplies video in separate (five wire video RGBHS) video format. If you hook the VFX-M up to a multiscan monitor with a regular VGA cable then you will be giving RGBHS to the monitor. Be sure to not select sync-on-green in the VFX-M video parameters or you will get a green cast to the image.

4.5.1 Application Note: Adjusting the Timing Parameters

Rastergraf's GLP software allows you to define the timing parameters in one of two ways:

a) the simple way, wherein you tell GLP that you are using a multiscan monitor. You specify the display active width and height (e.g. 1600 x 1280) and the Vertical Frequency, and the program figures out the rest.

b) the complete way, wherein you tell GLP exactly what you want the timing to be. You specify:

- vertical frequency in Hz
- vertical blanking in milliseconds (ms)
- vertical front porch in ms
- vertical sync width in ms
- horizontal blanking in microseconds (μs)
- horizontal front porch in μs
- horizontal sync width in μs
- display width and height

The program derives the horizontal frequency from this information.

Ordinarily, you should be able to use the monitor's data sheet to obtain a satisfactory display. However, it may be that adjustments are required. This section gives you some advice on how to do this. You can also supply Rastergraf with a filled-in copy of the monitor parameters sheet which follow this section. We can then assist you in solving your display problem.

Most monitors have adjustments for Horizontal Frequency, Horizontal Position, Horizontal Size, Vertical Frequency, Vertical Position and Vertical Size. It is recommended that the monitor adjustments be tried before trying monitor settings not in accord with the monitor data sheet.

To change the horizontal frequency:

The horizontal frequency is also known as horizontal refresh rate or horizontal scan rate. Indications that the horizontal frequency needs to be changed are an unviewable picture with diagonal lines. Some monitors display no picture when the horizontal frequency is out of its bandwidth. The same symptoms can be caused by no sync at all, so make sure that the cables are connected correctly and that the monitor is configured correctly.

When the picture is out of sync, the number of diagonal lines is an indication of how close to the correct horizontal frequency you are: fewer lines are closer, more lines are farther. Remember that changing the horizontal frequency will also affect the vertical frequency. Decreasing the horizontal frequency will generally result in a wider picture.

To change the horizontal position:

To shift the image *left* **increase** the horizontal front porch by the same amount. Perform the converse procedure to move the image to the *right*.

To change the width of the image:

There are 2 ways to change the width (horizontal size) of the image.

1) Display more pixels. The aspect ratio remains the same.

2) Change the ***vertical*** frequency. GLP derives the horizontal frequency from the other parameters. Increasing the horizontal frequency will result in a wider image, decreasing it will result in a narrower image.

To change the vertical frequency:

The vertical frequency is also known as vertical refresh rate or vertical scan rate. Indications that the vertical frequency needs to be changed are a picture which rolls up or down. Sometimes the appearance is of multiple pictures, one on top of another, with multiple horizontal lines. An excessively slow vertical frequency will cause the image to flicker. Some monitors display no picture when the vertical frequency is out of its bandwidth. Since the same symptoms can be caused by no sync at all, make sure that the cables are connected correctly and that the monitor is configured correctly.

To change the vertical position:

To shift the image *up* **increase** the vertical front porch by the same amount. Perform the converse procedure to move the image *downward*.

To change the height of the image:

There are 2 ways to change the height (vertical size) of the image.

1) Display more lines. The aspect ratio remains the same.

2) Change the vertical frequency. Increasing the vertical frequency will result in a shorter image, decreasing it will result in a taller image.

Declaration

Rastergraf is dedicated to making your application work. We can assist in determining special video timing parameters for specific monitors and other output devices. If you need help it would be very useful if you can gather the data requested in the following form before calling us.

4.5.2 Pan and Scroll

Panning and scrolling are techniques used to provide a window into a larger memory than can be displayed. This method is also called roaming. The display X (pan) and Y (scroll) starting points are changed, allowing new data areas to be displayed. This function is appropriate on the VFX-M when using a display format which doesn't use up all of memory. For example, a display 1280 x 1024 x 8 bpp gives you a little more than three full screens to roam around in with a VFX-M that has 4 MB VRAM. Routines in the Rastergraf software provide you with an easy way to pan and scroll in memory.

Request for Assistance in Determining Video Timing Parameters

Submit to: Rastergraf Inc.
1804-P SE First Street
Redmond, OR 97756 USA
TEL: (541) 923-5530
FAX: (541) 923-6475
email: support@rastergraf.com

Company Information
Company Name_____
Contact_____
Phone Number_____
Fax Number_____
email_____

Monitor Information
Monitor Brand_____ Model Number_____

VFX-M Information
Model Number_____ Serial Number_____

Horizontal Timing Information
Note: Horizontal timings may be given in pixel units (if given) or time units.
Horizontal Pixels per Line Displayed_____
Pixel Time or Frequency (optional)_____
Horizontal Total Line Time or Frequency_____
Horizontal Front Porch_____
Horizontal Sync Width_____
Horizontal Back Porch_____

Vertical Timing Information
Note: Vertical timings may be given in line units or time units.
Vertical Lines Displayed_____ Interlaced? (Yes/No)_____
Vertical Lines Total or Frequency (Field Rate)_____
Vertical Lines Total or Frequency (Frame Rate)_____
(same as Field Rate unless interlaced)
Vertical Front Porch_____
Vertical Sync Width_____
Vertical Back Porch_____

Sync Information
Sync Polarity (+ or -): Composite:_____ Horizontal:_____ Vertical:_____

Additional Notes
_____
_____
_____

Table 4-8 VFX-M Video Timing Parameter Request Form

4.6 VFX-M Interrupts

There is not a lot to say about interrupts for the VFX-M. The I128S2 is connected to the INTA line. The interrupt is controlled through the I128S2.

What happens on that line at the other end (CPU side) is beyond the scope of this manual. In most cases, the interrupts are combined with other PCI slots, and the software will have to poll all PCI devices to see who made the interrupt. In some computers, such as Alphas, each PCI slot has unique PCI interrupt lines, so that it is easier to isolate down to the slot what the interrupting device is.

4.7 Flash EEPROM

The VFX-M has a location for installing a 128 KB Flash EEPROM.

The code in the PROM cannot be directly executed. It must be read by the host CPU into its memory and executed from there. The I128S2 accesses the PROM data through the Mask Buffer data port, which is also used to access the RAMDAC and Auxiliary Control Registers.

The multiplexed Mask Buffer DRAM address bits contain both the high and low order address lines for the PROM. The high order lines appear first and so must be latched externally. In the table below, LMA refers to latched addresses, MAD refers to the low order lines which don't have to be latched.

Although in most cases the standard BIOS PROM would be 64 KB, a 128 KB is used on the VFX-M due to a bug in the I128S2 which requires that the minimum PROM size be 128 KB.

The VFX-M has overlapping positions to accommodate 32, 40 and 48 pin devices. Since the address connections on all three devices don't match exactly, to simplify the layout some of the address lines have been redefined:

Table 4-9 Flash EEPROM Logical/Physical Address Mapping

PROM	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Logical	16	11	10	9	8	15	14	13	12	7	6	5	4	3	2	1	0
Physical (LMA)	10	17	13	12	--	15	11	14	16	-	-	-	-	-	-	-	-
Physical (MAD)	--	--	--	--	8	--	--	--	--	7	6	5	4	3	2	1	0

4.8 Serial EEPROM

The graphics board includes an IC position for an Atmel AT24C02 (or equivalent) 2 Kb (256 bytes) I^2C Serial Electrically Erasable Programmable Read Only Memory (EEPROM). The programming of the Serial EEPROM is done through control lines on the I128S2.

I128S2 Signal Name	EEPROM Mnemonic	Description
DC_CLK	SCL	Serial EEPROM clock
DC_DAT	SDA	Serial EEPROM data input/output

The EEPROM is programmed using the standard Philips I^2C two wire system. The protocol for programming the EEPROM is delineated in the I^2C Bus Specification: see Philips web site: http://www-eu.semiconductors.philips.com/acrobat/various/I2C_BUS_SPECIFICATION_2.pdf.

In general, the method for accessing the EEPROM is to use DC_CLK to clock commands and data into or out of the EEPROM, with data passed to the EEPROM over DC_DAT.

Serial EEPROM Data Format

Rastergraf reserves the first 128 bytes of the 256 byte Serial EEPROM for internal use. This includes the VFX-M board serial number, revision, and configuration data. The remaining 128 bytes are left for user data. The following table lists the byte assignments in the EEPROM.

Table 4-10 VFX-M Serial EEPROM Example Listing

EEPROM Address	EEPROM Data	Description
0x00 - 0x07	0x00	Reserved for Rastergraf Use Only
0x08	0x01	VFX-M Serial EEPROM Data Format
0x09-0x0F	0x??	Board Serial Number in ASCII
0x10	0x01	VFX-M Board ID
0x11	0x??	VFX-M Fab Rev (0xFF = rev unknown)
0x12	0x??	VFX-M Configuration Code Bit 0 = reserved Bit 1 = Low 4 MB VRAM installed Bit 2 = High 4 MB VRAM installed Bit 3 = 64 MB DRAM installed Bit 4 = Mask Buffer DRAM installed Bit 5-7 = reserved
0x13	0x03	VFX-M Software Configuration Code Bit 0 = VGA BIOS installed Bit 1 = FCODE BIOS installed Bit 2-7 = Reserved
0x14-0x1F	0x00	Reserved for Rastergraf Use Only
0x20-0x7F	0x??	Soft configuration
0x80-0xFF	0x??	128 bytes available for customer use

Soft Configuration

The soft configuration array is a sequence of the following entries.

Entry	to	Entry		Units
0x0			0x??	Name length
0x1		nlen	0x??	Name
nlen+1			0x??	Data length
nlen+2		nlen+dlen+1	0x??	Data

For the last entry the name length is zero.

Soft configuration will only be used by BIOS code to setup a default video configuration. GLP does not use the Soft Configuration Data (SCD) directly to control video mode programming. However, the SCD can be accessed from GLP via the pk_get_attribute and pk_set_attribute calls. The following soft configuration variables are defined:

General video parameters

Name	Description	Units
w	width	pixels (640 default)
h	height	pixels (480 default)
p	pixel format	8 (default), 16, 555, or 24
f	vertical sync frequency	Hz (60 default)
P	pitch	pixels (default to width)

Video timing override

Name	Description	Units
pf	Pixel frequency	MHz
hf	Horizontal frequency	KHz
hp	Horizontal front porch	microseconds
hs	Horizontal sync	microseconds
hb	Horizontal blanking	microseconds
vp	Vertical front porch	milliseconds
vs	Vertical sync	milliseconds
vb	Vertical blanking	milliseconds

Register Override *

Name	Description	Values
Wxx	RBASE_W register override	32-bit (hex)
Gxx	RBASE_G register override	32-bit (hex)
Dxx	RBASE_D register override	32-bit (hex)
Cxx	RBASE_C register override	32-bit (hex)
Ixx	RBASE_I register override	32-bit (hex)
Oxx	IO register override	32-bit (hex)
Rxx	RAMDAC register override	byte (hex)

*** Note: Name** denotes an offset (in hex) from the RBASE_n or RAMDAC base register address.

Chapter 5
Troubleshooting

Introduction

This chapter contains information which should assist you in tracking down installation and functional problems with your board.

5.1 General procedures

5.2 Dealing with the PCI bus

5.3 Maintenance, Warranty, and Service

5.1 General Procedures

The VFX-M boards were designed with reliability and durability in mind. Nevertheless, it may happen that a problem will occur. This section is devoted to aiding the user in tracking down the problem efficiently and quickly.

You may be able to locate minor problems without technical assistance. Before placing a service call, try to solve the problem by following the directions given below, in Table 5-1. If the problem can not be remedied, Rastergraf can then issue a Return Material Authorization (RMA) so that the board can be returned to the factory for quick repair.

It can happen that installing a new board will overload the computer's power supply if the power supply margins are exceeded. The first step in ascertaining if this is the problem is to calculate a power supply budget. This involves adding up the power requirements of each board in the system to see if you are within specification. Consult your computer's technical manual for information on how to correctly determine this. A typical VFX-M will draw about 1.5 amps at +5 volts.

When attempting to verify that the power supply is working properly, it is not unusual to unplug everything and measure the supply without a load. While this practice is acceptable for linear supplies, switching supplies (which are very commonly used in computers) require a certain load before proper regulation is achieved. Typically, at least 5 Amps must be drawn from the +5 volt supply before the +12 volt supplies will give the proper readings.

It can also happen that if you build your own cables and you short +5 to ground on the VFX-M front panel connector you may trigger the auto-resetting fuse which protect power supply pins when an overload occurs. The fuse resets automatically when an overload is removed.

Table 5-1 Basic Troubleshooting procedures

Fault	Possible Cause	Corrective Action
Control Panel dead - On/Off switch unlit	No AC power	Check power cord. It may have been dislodged when installing board.
On/Off Switch lit	No DC power	Check for correct +5 and +12 volts.
Cannot Boot	Cable(s) dislodged	During installation an unrelated cable can get dislodged.
Cannot read Rastergraf distribution media	Improperly inserted, damaged, or incorrect media.	Check insertion and position. Take care that media is “mounted” properly. Unix distribution uses TAR format.
No message on console terminal or messages are garbled	Terminal disconnected or not configured properly.	Make sure cable between terminal and computer is plugged into proper terminal port. Put terminal into Local mode and verify operation.
System crashes or you get a “Trap” message	Software not installed correctly	Check installation procedures. See Software Release Notes.
No image on Monitor	COAX cables not connected properly or monitor is not on.	Check cables, replace if necessary. Be sure to initialize board with correct initialization parameters.
Image is smeared or doing flip-flops	Sync signals missing or monitor sync failure.	Make sure monitor accepts sync on green, that monitor is terminated, and the hold controls are adjusted properly. Check video timing parameters.
PX Windows Server is very slow to start up. Mouse movement is fast but windows are slow to open.	Graphics board to Host CPU interrupts are not being serviced.	Check interrupt pass/grant jumpers. Check operating system for correct interrupt configuration.
No response to mouse motion and/or keyboard entry.	Keyboard or mouse cable not plugged in. PX Windows board side server is crashed.	Check cabling. Reload software.
VFX-M not detected by BIOS firmware or Operating System.		a) Check BIOS configuration b) Check board seating c) Check driver installation.

5.2 Dealing with the PCI Bus

Because of the nature of the PCI protocol and the way support has been implemented in the Operating Systems for PCI bus devices such as the VFX-M, it is not possible to follow the same debugging strategies.

In fact, there are no address jumpers for these boards. Everything is configured in software through a set of on-board registers, which control the characteristics of the board as required by the PCI Specification.

The information used to program these registers is supplied to Operating System (OS) specific functions by Rastergraf's software. Ordinarily, several address map translations occur, including the CPU physical and virtual address maps and the CPU to PCI bridge address map.

The result of this is that the operation of the VFX-M is very sensitive to the host CPU, as no standards have been adopted which guarantee, or even imply, universality among CPU boards, even if they use the same CPU and PCI bridge. Therefore, it is vital to ensure that Rastergraf can vouch for the board's operation in a particular CPU before you go crazy trying to figure out why it doesn't. Please contact us (support@rastergraf.com or 541-923-5530) if you have problems.

5.3 Maintenance, Warranty, and Service

Maintenance

The VFX-M requires no regular service, but if used in a particularly dirty environment, periodic cleaning with dry compressed air is recommended.

Because of the heat generated by normal operation of the graphics board and other boards in the system, forced crossflow ventilation is required. If forced ventilation is not used IC temperatures can rise to 60 degrees C or higher. Such high temperature operation causes IC failures and reduced MTBF. With proper forced air cooling IC temperatures will be less than 35 degrees C.

Warranty

The VFX-M graphics boards are warranted to be free from defects in material or manufacture for a period of 1 year from date of shipment from the factory. Rastergraf's obligation under this warranty is limited to replacing or repairing (at its option) any board which is returned to the factory within this warranty period and is found by Rastergraf to be defective in proper usage. This warranty does not apply to modules which have been subjected to mechanical abuse, electrical abuse, overheating, or other improper usage. This warranty is made in lieu of all other warranties expressed or implied. **All warranty repair work will be done at the Rastergraf factory.**

Return Policy

Before returning a module the customer must first request a Return Material Authorization (RMA) number from the factory. The RMA number must be enclosed with the module when it is packed for shipment. A written description of the trouble should also be included.

Customer should prepay shipping charges to the factory. Rastergraf will prepay return shipping charges to the customer. Repair work is normally done within ten working days from receipt of module.

Out of Warranty Service

Factory service is available for modules which are out of warranty or which have sustained damage making them ineligible for warranty repair. A flat fee will be charged for normal repairs and must be covered by a valid purchase order. If extensive repairs are required, Rastergraf will request authorization for an estimated time and materials charge. If replacement is required, additional authorization will be requested.

All repair work will be done at the Rastergraf factory in Redmond, Oregon, unless otherwise designated by Rastergraf.

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