

PMB-C

User's Manual

Dual PMC Carrier for 6U CompactPCI
with Front and Rear Panel I/O

Rastergraf

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Release 3.0
March 5, 2008

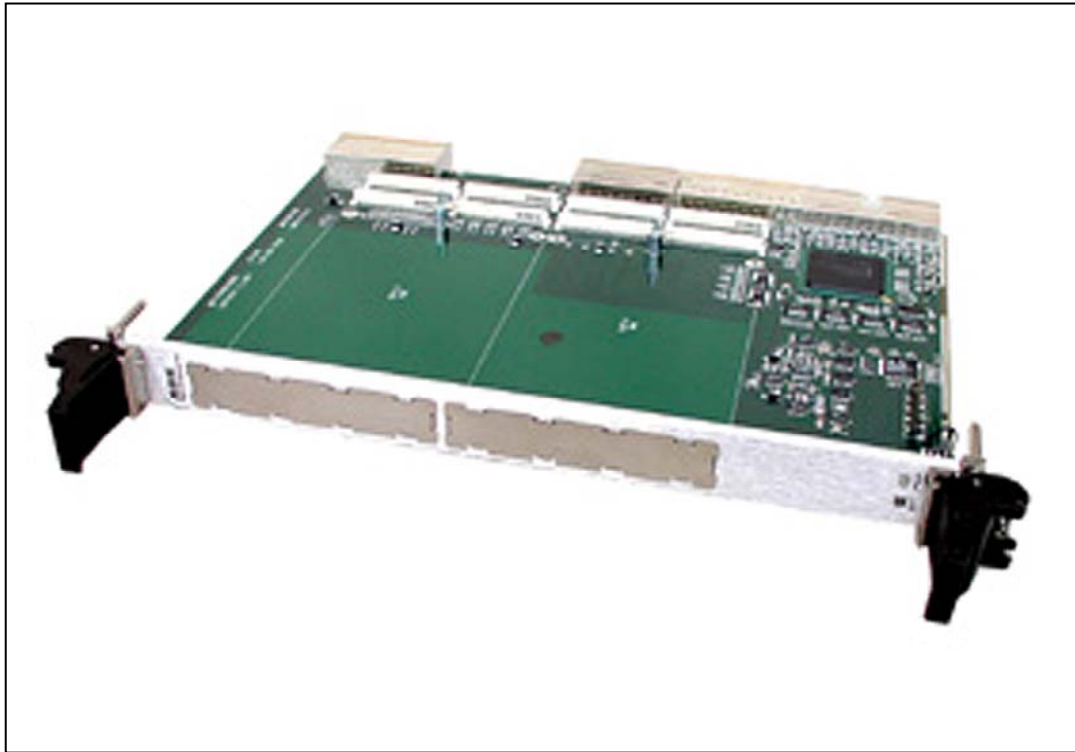
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Introduction

This manual provides information about how to configure, install, and program the Rastergraf PMB-C Dual PMC Carrier for 6U 32-bit and 64-bit CompactPCI Computers.

This manual is broken down into four chapters:

- Chapter 1: General Information
- Chapter 2: Installing the PMB-C
- Chapter 3: Programming Devices
- Chapter 4: Troubleshooting

Chapter 1 provides background material about the PMB-C board. Understanding the information in the chapter, however, is not essential for the hardware or software installation. If you want to perform the installation as quickly as possible, start with Chapter 2. If you have problems installing the hardware, refer to Chapter 4 for help.

Getting Help

This installation manual gives specific steps to take to install your Rastergraf board. There are, however, variables specific to your computer configuration and monitor that this manual cannot address. Normally, the default values given in this manual will work. If you have trouble installing or configuring your system, first read Chapter 6, “Troubleshooting”. If this information does not enable you to solve your problems, do one of the following:

- 1) call Rastergraf technical support at (541) 923-5530
- 2) fax your questions to (541) 923-6475
- 3) send E-mail to support@rastergraf.com.

Board Revisions

This manual applies to the following board revision levels:

PMB-C All revisions

Manual Revisions

Revision 1.3	May 22, 2002	First released version
Revision 1.4	August 7, 2002	Added Solaris Hotswap info
Revision 1.5	September 11, 2002	Corrected CPCI J5 Pinout
Revision 1.6	December 11, 2002	Un-corrected CPCI J5 Pinout. It was right before ☺
Revision 2.0	March 4, 2008	Rastergraf version

Notices

Information contained in this manual is disclosed in confidence and may not be duplicated in full or in part by any person without prior approval of Rastergraf. Its sole purpose is to provide the user with adequately detailed documentation to effectively install and operate the equipment supplied. The use of this document for any other purpose is specifically prohibited.

The information in this document is subject to change without notice. The specifications of the PMB-C PMC Carrier board and other components described in this manual are subject to change without notice. Although it regrets them, Rastergraf assumes no responsibility for any errors or omissions that may occur in this manual. Customers are advised to verify all information contained in this document.

The electronic equipment described herein generates, uses, and may radiate radio frequency energy, which can cause radio interference. Rastergraf assumes no liability for any damages caused by such interference.

Rastergraf products are **not** authorized for **any** use as critical components in flight safety or life support equipment without the written consent of the president of Rastergraf, Inc.

These products have been designed to operate in user-provided PMC-compatible computers. Connection of incompatible hardware is likely to cause serious damage. Rastergraf assumes no liability for any damages caused by such incompatibility.

Rastergraf assumes no responsibility for the use or reliability of software or hardware that is not supplied by Rastergraf, or which has not been installed in accordance with this manual.

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Conventions Used In This Manual

The following list summarizes the conventions used throughout this manual.

Code fragments	Code fragments, file, directory or path names and user/computer dialogs in the manual are presented in the <code>courier</code> typeface.
Commands or program names	Commands, or the names of executable programs, except those in code fragments, are in bold.
System prompts and commands	Commands in code fragments are preceded by the system prompt, a percentage sign (%), the standard prompt in UNIX's C shell, or the hash-mark (#), the standard UNIX prompt for the Super-User.
Keyboard usage	<CR> stands for the key on your keyboard labeled "RETURN" or "ENTER"

Note	Note boxes contain information either specific to one or more platforms, or interesting, background information that is not essential to the installation.
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Caution	Caution boxes warn you about actions that can cause damage to your computer or its software.
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Warning!	Warning! boxes warn you about actions that can cause bodily or emotional harm.
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Chapter 1

General Information

1.1 Introduction

The Rastergraf PMB-C is part of Rastergraf's line of active and passive interface PMC carriers for PCI and CompactPCI computers

The PMB-C mezzanine carrier board holds two PMC modules with front or rear-panel I/O support in a single 6U CompactPCI slot. The PMB-C carrier board is ideal for use in high performance industrial, COTS, and telephony CompactPCI systems that require I/O expansion using the PMC module form factor.

Using the industry standard Intel 21154-BC PCI-to-PCI Bridge, the PMB-C supports a 64-bit data path at 66 MHz, for 512 MB/s operation. The PMC sites support bus mastering. The PMB-C carrier board complies with the PICMG 2.0, version 3.0 CompactPCI specification.

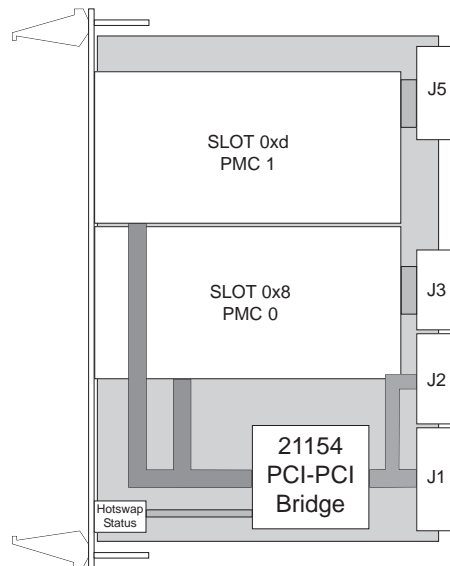
The PMB-C can be used with a PIM carrier to provide I/O through the CompactPCI J3 and J5 connectors. See Section 1.3 for more information.

For information about all of Rastergraf's products, please contact Rastergraf Worldwide Sales at (541) 923-5530 or, consult Rastergraf's web page at <http://www.rastergraf.com>.

1.2 Feature Summary

- 6U CompactPCI carrier board holds two PMC modules
- 64-bit, 33/66 MHz, up to 512 MB/s operation
- Full Hot Swap capability
- Status LEDs for Power (green) and Hot Swap (blue)
- Intel 21154-BC PCI to PCI Bridge
- Supports standard IEEE1386.1 PMC mezzanine modules
- CompactPCI specification, PICMG 2.0, version 3.0 compliant
- Front or rear panel I/O support for both PMC slots
- 128 I/O lines via rear panel J3 and J5 CompactPCI connectors
- 5V PCI signaling for the PMC sites.
- Optional 3.3V PCI signaling (contact factory)
- Compatibility with PIM Carrier (see Section 1.3)

Figure 1-1 PMB-C Block Diagram



SLOT	Module	Front Panel I/O Location	Rear Panel I/O Location	Bus Master
0	PMC	On module	J3	Yes
1	PMC	On module	J5	Yes

1.3 PIM Carrier

This manual is about the PMB-C dual PMC carrier, but an important accessory is the rear panel expansion capability.

The PIM Carrier provides two locations for PIM (PMC I/O Module) boards. It offers a standardized (VITA 36) way of making connections to PMC modules via the Rear Panel I/O (J4) connector which is part of the PMC four connector set. The combination of the PMB-C, PIM Carrier, and PIM expander modules makes a seamless path for many Rear Panel I/O requirements.

Rastergraf currently recommends the PIM Carrier products manufactured by Dynamic Engineering (http://www.dyneng.com/cpci.html#pim_carrier).

Figure 1-2 PMB-C Integration with a PIM Carrier

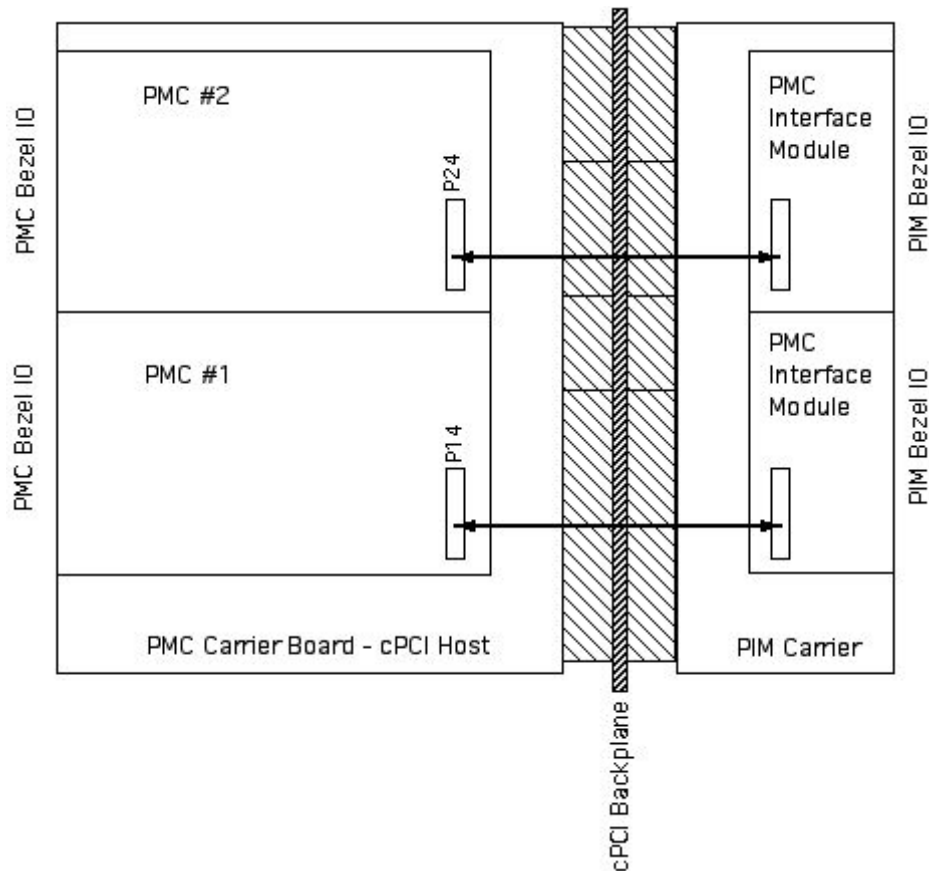


Figure 1-3 PIM Carrier

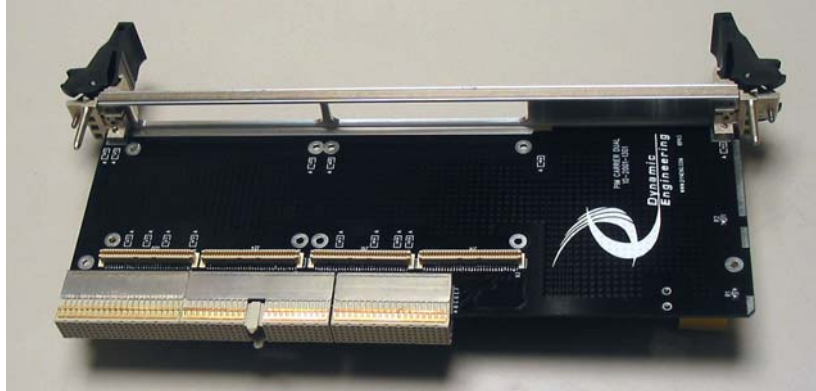
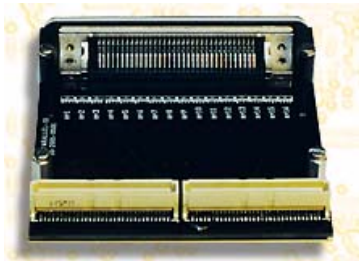


Figure 1-4 PIM Adapter Board



1.4 Additional References

You can find Rastergraf documentation and technical literature on the Rastergraf web page (<http://www.rastergraf.com>).

The *CompactPCI Specification – PICMG R2.0 R3.0*, the *CompactPCI Hot Swap Specification – PICMG 2.1 R2.0* and the *CompactPCI Hot Swap Infrastructure Interface Specification PICMG 2.12 R1.0* standards and other information are available from **PICMG**:

Web Page: <https://www.picmg.org/index.stm>

Comprehensive documentation about the *21154 PCI to PCI Bridge* is available from **Intel**:

Web Page: <http://developer.intel.com/design/bridge/>

The *PCI Local Bus 2.2 Specification* is maintained by the **PCI Special Interest Group** (PCISIG)

Web Page: <http://www.pcisig.com/home>

1.5 Specifications for the PMB-C

Form Factor:	6U CompactPCI
CompactPCI Bridge	Intel 21154-BC PCI to PCI Bridge, 32/64-bit, 33/66 MHz
CompactPCI Compatibility	PICMG 2.0 Rev 3, IEEE 1101.10, and PCI Specification Revision 2.2 compliant. 6U form factor w/ ESD strips
Hot Swap Support	PICMG 2.1 R1.0, Section 2.3.2.4. Uses “alternate register” method as defined in the CompactPCI Hot Swap Specification. The 21154-BC does not have a Hot Swap Control and Status register as part of its register set. Therefore it is not considered to be Hot Swap “silicon friendly”. This is not the kiss of death. Actually, it is very common in devices that claim hot-swap support.
PMC Device Access:	Programmable Bus Address Registers (BARs) in the 21154-BC map the two on-board PMC slots through its 32/64-bit, 33/66 MHz PCI interface.
CompactPCI Interrupts:	Interrupts from the PMC slots are mapped according the PCI Bridge Specification and are connected to the CompactPCI bus without going through the 21154-BC. See Section 3.2.4 for more information.
CompactPCI Bus Master	Two slots through a transparent bridge
CompactPCI Bus Loading:	One PCI 2.2 compatible load
I/O Access	Front and Rear Panel (PMC J4). PMC Slot 0 I/O goes to CPCI J3 and PMC Slot 1 goes to CPCI J5.
PCI Compatibility	PCI Specification, Revision 2.2 compliant
PMC Interface	Two IEEE 1386.1 PMC mezzanine modules
PIM Compatibility	VITA 36 – 199x standard for PMC I/O Module. Interoperates with PIM Carrier (see Section 1.3).

Power Requirements

+3.3 VDC, 600 mA max
+5 VDC, 100 mA max

Additional 3.3V and 5V power is consumed by the PMC modules. Power consumption is limited by PMB-C to 7.5W (total) per PMC site.

A Hot Swap controller chip channels power to the PMC slots through switching FETs. The Hot Swap controller limits the current to a total of 6.6 A for 3.3 V and 5.3 A for 5V for both PMC slots. Needless to say, this allows you to go way over the nominal 7.5W limit for each board, but please don't do it.

Dimensions

233 mm x 160 mm

Weight

0.26 kg (0.56 lb)

Environmental

Operating temperature: 0 to 70°C
Storage: -40 to +85°C
Humidity: 5 to 95% non-condensing

Environment:

Temperature: 0 to 70 degrees C, operating
-55 to +85 degrees C, storage
Humidity: 5% to 90%, non-condensing

1.6 PMB-C Connectors

Connector	Description	Section
J1	PCI Bridge	CompactPCI bus
J2	PCI Bridge	CompactPCI bus
J3	J14	Back-panel I/O for PMC slot 0 (0x8)
J5	J24	Back-panel I/O for PMC slot 1 (0xd)
J11, J12, J13	PCI Bridge	PCI bus for slot 0 (0x8)
J21, J22, J23	PCI Bridge	PCI bus for slot 1 (0xd)

1.6.1 CompactPCI Bus J1 Connector

Position	A	B	C	D	E	F
1	VCC (5V)	-12V	n/c	+12V	VCC (5V)	GND
2	n/c	VCC (5V)	n/c	TDOH	TDIH	GND
3	INTA#	INTB#	INTC#	VCC (5V)	INTD#	GND
4	n/c	HEALTHY#	VIO	n/c	n/c	GND
5	n/c	n/c	RST#	GND	GNT#	GND
6	REQ#	GND	VDD (3.3V)	CLK	AD[31]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
8	AD[26]	GND	VIO	AD[25]	AD[24]	GND
9	CBE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
10	AD[21]	GND	VDD (3.3V)	AD[20]	AD[19]	GND
11	AD[18]	AD[17]	AD[16]	GND	CBE[2]#	GND
12	keyway	keyway	keyway	keyway	keyway	keyway
13	keyway	keyway	keyway	keyway	keyway	keyway
14	keyway	keyway	keyway	keyway	keyway	keyway
15	VDD (3.3V)	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
16	DEVSEL#	GND	VIO	STOP#	LOCK#	GND
17	VDD (3.3V)	n/c	n/c	GND	PERR#	GND
18	SERR#	GND	VDD (3.3V)	PAR	CBE[1]#	GND
19	VDD (3.3V)	AD[15]	AD[14]	GND	AD[13]	GND
20	AD[12]	GND	VIO	AD[11]	AD[10]	GND
21	VDD (3.3V)	AD[09]	AD[08]	M66EN	CBE[0]#	GND
22	AD[07]	GND	VDD (3.3V)	AD[06]	AD[05]	GND
23	VDD (3.3V)	AD[04]	AD[03]	VCC (5V)	AD[02]	GND
24	AD[01]	VCC (5V)	VIO	AD[00]	ACK64#	GND
25	VCC (5V)	REQ64#	ENUM#	VDD (3.3V)	VCC (5V)	GND

signal Indicates PMB-C pins which connect to Long Hot Swap backplane pins

signal Indicates PMB-C pins which connect to Short Hot Swap backplane pins

1.6.2 CompactPCI Bus J2 Connector

Position	A	B	C	D	E	F
1	n/c	GND	n/c	n/c	n/c	GND
2	n/c	n/c	n/c	n/c	n/c	GND
3	n/c	GND	n/c	n/c	n/c	GND
4	VIO	GND	C/BE[7]#	GND	C/BE[6]#	GND
5	C/BE[5]#	64EN#	VIO	C/BE[4]#	PAR64	GND
6	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
7	AD[59]	GND	VIO	AD[58]	AD[57]	GND
8	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
9	AD[52]	GND	VIO	AD[51]	AD[50]	GND
10	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
11	AD[45]	GND	VIO	AD[44]	AD[43]	GND
12	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
13	AD[38]	GND	VIO	AD[37]	AD[36]	GND
14	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
15	n/c	GND	n/c	n/c	n/c	GND
16	n/c	n/c	n/c	GND	n/c	GND
17	n/c	GND	n/c	n/c	n/c	GND
18	n/c	n/c	n/c	GND	n/c	GND
19	n/c	n/c	n/c	n/c	n/c	GND
20	n/c	n/c	n/c	GND	n/c	GND
21	n/c	n/c	n/c	n/c	n/c	GND
22	PU-VIO	PU-VIO	PU-VIO	PU-VIO	PU-VIO	GND

1.6.3 CompactPCI Bus J3 Connector to PMC Slot 0 (0x8)

Position	A	B	C	D	E	F
1	S_VI/O	PMC0_IO64	PMC0_IO63	PMC0_IO62	PMC0_IO61	GND
2	PMC0_IO60	PMC0_IO59	PMC0_IO58	PMC0_IO57	PMC0_IO56	GND
3	PMC0_IO55	PMC0_IO54	PMC0_IO53	PMC0_IO52	PMC0_IO51	GND
4	PMC0_IO50	PMC0_IO49	PMC0_IO48	PMC0_IO47	PMC0_IO46	GND
5	PMC0_IO45	PMC0_IO44	PMC0_IO43	PMC0_IO42	PMC0_IO41	GND
6	PMC0_IO40	PMC0_IO39	PMC0_IO38	PMC0_IO37	PMC0_IO36	GND
7	PMC0_IO35	PMC0_IO34	PMC0_IO33	PMC0_IO32	PMC0_IO31	GND
8	PMC0_IO30	PMC0_IO29	PMC0_IO28	PMC0_IO27	PMC0_IO26	GND
9	PMC0_IO25	PMC0_IO24	PMC0_IO23	PMC0_IO22	PMC0_IO21	GND
10	PMC0_IO20	PMC0_IO19	PMC0_IO18	PMC0_IO17	PMC0_IO16	GND
11	PMC0_IO15	PMC0_IO14	PMC0_IO13	PMC0_IO12	PMC0_IO11	GND
12	PMC0_IO10	PMC0_IO9	PMC0_IO8	PMC0_IO7	PMC0_IO6	GND
13	PMC0_IO5	PMC0_IO4	PMC0_IO3	PMC0_IO2	PMC0_IO1	GND
14	VDD (3.3V)	VDD (3.3V)	VDD (3.3V)	VCC (5V)	VCC (5V)	GND
15	n/c	n/c	n/c	n/c	n/c	GND
16	n/c	n/c	n/c	n/c	n/c	GND
17	n/c	n/c	n/c	n/c	n/c	GND
18	n/c	n/c	n/c	n/c	n/c	GND
19	n/c	n/c	n/c	n/c	n/c	GND

1.6.4 CompactPCI Bus J5 Connector to PMC Slot 1 (0xd)

Position	A	B	C	D	E	F
1	S_VI/O	PMC1_IO64	PMC1_IO63	PMC1_IO62	PMC1_IO61	GND
2	PMC1_IO60	PMC1_IO59	PMC1_IO58	PMC1_IO57	PMC1_IO56	GND
3	PMC1_IO55	PMC1_IO54	PMC1_IO53	PMC1_IO52	PMC1_IO51	GND
4	PMC1_IO50	PMC1_IO49	PMC1_IO48	PMC1_IO47	PMC1_IO46	GND
5	PMC1_IO45	PMC1_IO44	PMC1_IO43	PMC1_IO42	PMC1_IO41	GND
6	PMC1_IO40	PMC1_IO39	PMC1_IO38	PMC1_IO37	PMC1_IO36	GND
7	PMC1_IO35	PMC1_IO34	PMC1_IO33	PMC1_IO32	PMC1_IO31	GND
8	PMC1_IO30	PMC1_IO29	PMC1_IO28	PMC1_IO27	PMC1_IO26	GND
9	PMC1_IO25	PMC1_IO24	PMC1_IO23	PMC1_IO22	PMC1_IO21	GND
10	PMC1_IO20	PMC1_IO19	PMC1_IO18	PMC1_IO17	PMC1_IO16	GND
11	PMC1_IO15	PMC1_IO14	PMC1_IO13	PMC1_IO12	PMC1_IO11	GND
12	PMC1_IO10	PMC1_IO9	PMC1_IO8	PMC1_IO7	PMC1_IO6	GND
13	PMC1_IO5	PMC1_IO4	PMC1_IO3	PMC1_IO2	PMC1_IO1	GND
14	n/c	n/c	n/c	n/c	n/c	GND
15	n/c	n/c	n/c	n/c	n/c	GND
16	n/c	n/c	n/c	n/c	n/c	GND
17	n/c	n/c	n/c	n/c	n/c	GND
18	n/c	n/c	n/c	n/c	n/c	GND
19	n/c	n/c	n/c	n/c	n/c	GND
20	n/c	n/c	n/c	n/c	n/c	GND
21	n/c	n/c	n/c	n/c	n/c	GND
22	n/c	n/c	n/c	n/c	n/c	GND

1.6.5 PMC Bus Connectors – J1

Pin	Notes	Signal Name	Signal Name	Notes	Pin
1	PD	TCK	-12V		2
3		GND	INTAL		4
5		INTBL	INTCL		6
7	N/C	BUSMODEIL	VCC (5V)		8
9		INTDL	PCI-RSVD	N/C	10
11		GND	PCI-RSVD	N/C	12
13		PCICLK	GND		14
15		GND	PMCGNTL		16
17		PMCREQL	VCC (5V)		18
19		Vio	AD31H		20
21		AD28H	AD27H		22
23		AD25H	GND		24
25		GND	C/BE3L		26
27		AD22H	AD21H		28
29		AD19H	VCC (5V)		30
31		Vio	AD17H		32
33		FRAMEL	GND		34
35		GND	IRDYL		36
37		DEVSELL	VCC (5V)		38
39		GND	LOCK#		40
41	PU	SDONE#	SBO#	PU	42
43		PAR	GND		44
45		Vio	AD15H		46
47		AD12H	AD11H		48
49		AD09H	VCC (5V)		50
51		GND	C/BE0L		52
53		AD06H	AD05		54
55		AD04H	GND		56
57		Vio	AD03H		58
59		AD02H	AD01H		60
61		AD00H	VCC (5V)		62
63		GND	REQ64#	PU	64

Note: PD means pull down resistor to ground. PU means pull up resistor to VCC or VDD

1.6.6 PMC Bus Connectors – J2

Pin	Notes	Signal Name	Signal Name	Notes	Pin
1		+12V	TRSTL	PD	2
3	PU	TMSH	TDOH	N/C	4
5	N/C	TDIH	GND		6
7		GND	PCI_RSVD	N/C	8
9	N/C	PCI_RSVD	PCI_RSVD	N/C	10
11	PU	BUSMODE2L	VDD (3.3V)		12
13		PCIRSTL	BUSMODE3L	GND	14
15		VDD (3.3V)	BUSMODE4L	GND	16
17	N/C	PCI_RSVD	GND		18
19		AD30H	AD29H		20
21		GND	AD26H		22
23		AD24H	VDD (3.3V)		24
25		IDSEL	AD23H		26
27		VDD (3.3V)	AD20H		28
29		AD18H	GND		30
31		AD16H	C/BE2L		32
33		GND	PMC_RSVD	N/C	34
35		TRDYL	VDD (3.3V)		36
37		GND	STOPL		38
39		PERRL	GND		40
41		VDD (3.3V)	SERRL		42
43		C/BE1L	GND		44
45		AD14	AD13H		46
47		GND	AD10H		48
49		AD08H	VDD (3.3V)		50
51		AD07H	PMC_RSVD	N/C	52
53		VDD (3.3V)	PMC_RSVD	N/C	54
55	N/C	PMC_RSVD	GND		56
57	N/C	PMC_RSVD	PMC_RSVD	N/C	58
59		GND	PMC_RSVD	N/C	60
61	N/C	ACK64L	VDD (3.3V)		62
63		GND	PMC_RSVD	N/C	64

Note: PD means pull down resistor to ground. PU means pull up resistor to VCC or VDD

1.6.7 PMC Bus Connectors – J3

Pin	Notes	Signal Name
1	N/C	PMC-RSVD
3		GND
5		C/BE6L
7		C/BE4L
9		Vio
11		AD63H
13		AD61H
15		GND
17		AD59H
19		AD57H
21		Vio
23		AD55H
25		AD53H
27		GND
29		AD51H
31		AD49H
33		GND
35		AD47H
37		AD45H
39		Vio
41		AD43H
43		AD41H
45		GND
47		AD39H
49		AD37H
51		GND
53		AD35H
55		AD33H
57		Vio
59	N/C	PMC-RSVD
61	N/C	PMC-RSVD
63		GND

Signal Name	Notes	Pin
GND		2
C/BE7L		4
C/BE5L		6
GND		8
PAR6H4		10
AD62H		12
GND		14
AD60H		16
AD58H		18
GND		20
AD56H		22
AD54H		24
GND		26
AD52H		28
AD50H		30
GND		32
AD48H		34
AD46H		36
GND		38
AD44H		40
AD42H		42
GND		44
AD40H		46
AD38H		48
GND		50
AD36H		52
AD34H		54
GND		56
AD32H		58
PMC-RSVD	N/C	60
GND		62
PMC-RSVD	N/C	64

1.6.8 PMC Bus Connectors – J4

Pin	Signal Name	Signal Name	Pin
1	PMCx_IO1	PMCx_IO2	2
3	PMCx_IO3	PMCx_IO4	4
5	PMCx_IO5	PMCx_IO6	6
7	PMCx_IO7	PMCx_IO8	8
9	PMCx_IO9	PMCx_IO10	10
11	PMCx_IO11	PMCx_IO12	12
13	PMCx_IO13	PMCx_IO14	14
15	PMCx_IO15	PMCx_IO16	16
17	PMCx_IO17	PMCx_IO18	18
19	PMCx_IO19	PMCx_IO20	20
21	PMCx_IO21	PMCx_IO22	22
23	PMCx_IO23	PMCx_IO24	24
25	PMCx_IO25	PMCx_IO26	26
27	PMCx_IO27	PMCx_IO28	28
29	PMCx_IO29	PMCx_IO30	30
31	PMCx_IO31	PMCx_IO32	32
33	PMCx_IO33	PMCx_IO34	34
35	PMCx_IO35	PMCx_IO36	36
37	PMCx_IO37	PMCx_IO38	38
39	PMCx_IO39	PMCx_IO40	40
41	PMCx_IO41	PMCx_IO42	42
43	PMCx_IO43	PMCx_IO44	44
45	PMCx_IO45	PMCx_IO46	46
47	PMCx_IO47	PMCx_IO48	48
49	PMCx_IO49	PMCx_IO50	50
51	PMCx_IO51	PMCx_IO52	52
53	PMCx_IO53	PMCx_IO54	54
55	PMCx_IO55	PMCx_IO56	56
57	PMCx_IO57	PMCx_IO58	58
59	PMCx_IO59	PMCx_IO60	60
61	PMCx_IO61	PMCx_IO62	62
63	PMCx_IO63	PMCx_IO64	64

Chapter 2

Installing Your PMB-C Board

2.1 Introduction

Using the PMB-C necessarily involves some system integration issues. The PMB-C is a carrier for PMC cards, so, of course, you have to know what you are putting on the PMB-C.

It is beyond the scope of this manual to deal with selection and use of PMC modules, solving I/O problems, or software except as it relates to the 21154. However, the manual does address PMC board installation and suggests sources for PIM Carrier and Modules.

There are several steps involved in getting your PMB-C board to work in your system.

- Unpack the PMB-C board
- Install the PMC modules
- Install the PMB-C board

2.2 Unpacking Your Board

When you unpack your board, inspect the contents to see if any damage occurred in shipping. If there has been physical damage, file a claim with the carrier at once and contact Rastergraf for information regarding repair or replacement. Do not attempt to use damaged equipment.

Caution

Be careful not to remove the board from its antistatic bag or container until you are ready to install it. It is preferable to wear a grounded wrist strap whenever handling computer boards.

2.3 Preparing for Installation

Local PCI Bus Signaling Level

The PMB-C local PCI bus (the bus between the PMC boards and the 21154) can be operated either at 3.3V or 5V signaling, which determines the voltage level for a “high” or “one” in the PCI bus signal transitions.

The original PCI specification required 33 MHz systems to use 5V signaling and 66 MHz systems to use 3.3V in order to improve system performance and because 3.3V devices connected to a 5V bus would often fail. However, most current ICs are 5V tolerant and do not require the bus to be set to 3.3V for any reason.

The PMB-C can be jumpered to run the local bus at 3.3V. Because it is not ordinarily a user-installable jumper, please contact the factory should you wish to make this change.

2.4 PMC Board Installation

The PMB-C provides two single-wide PMC 32 or 64-bit, 33 or 66 MHz IEEE 1386-2001 compatible locations. You can install your PMC module in either of the available locations. The slots accept any standard PMC or CCPMC module. A Processor PMC (PPMC) card most likely will *not* work correctly with in the PMB-C because of the extra signals that the PPMC expects.

The PMB-C supports I/O either from the front panel using connectors mounted on the PMC card or from the rear of the computer via the path provided by the interconnection of PMC J4 connector, PMB-C J3 or J5, and a PIM carrier or other rear panel I/O adapter.

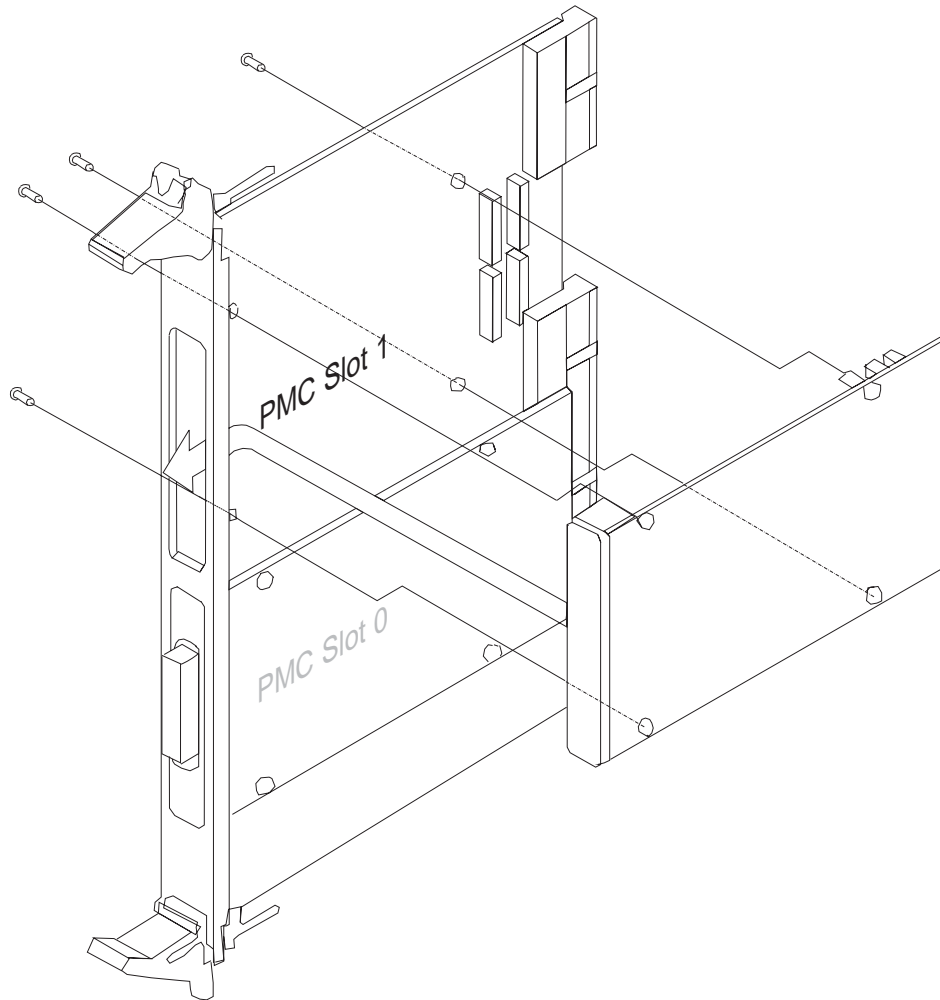
Warning!

If your PMC module requires 3.3V PCI signaling (this is *not* the same as 3.3V power) and will not work with 5V signaling (but most boards do) please contact the factory for assistance. Do not attempt to use your board with the PMB-C because it is normally set up for 5V signaling.

Installing the PMC Board

1. If you just received it, unpack your PMB-C and place it component side up on a clean anti-static surface.
2. Referring to Section 2.2, make sure that any jumpers or other changes to the PMB-C card are made now.
3. Make sure that any jumpers or other changes to the PMC card are made now.
4. Determine whether you are going to use front or rear panel I/O, and if the PMC card requires a special setting for your choice.
5. If you are using rear panel I/O, make sure you have a rear panel I/O adapter such as a PIM Carrier and the necessary PIM adapter card.
6. Identify an empty PMC location on the PMB-C. In general, it is good practice to start with PMC slot 0, but it is not required that you do so.

Figure 2-1 Installation of a PMC Module into the PMB-C



7. Note that the PMB-C does not have 5V or 3.3V signaling key pins installed because it is assumed that your PMC boards will work with 5V signaling (not to be confused with the power supply voltages). If your PMC board will not work with 5V signaling, go no further. Please contact the factory
8. Otherwise, insert the PMC card as shown in the figure above and secure it with the mounting screws.

Now, go to Section 2.5.

2.5 Installing the PMB-C

The PMB-C board can plug into any 32 or 64-bit, 5V or 3.3V signaling CompactPCI 6U slot.

Note:

Refer to *Section 2.4* for the instructions for installing PMC boards.

1. Shut down the operating system and **turn off the power**.

Warning!

Never open the computer without turning off the power supply. Unless internal AC wiring is exposed, leave the power cord plugged in, so as to ground the computer chassis. You can easily get shocked, ruin computer parts or both unless you turn off the power. Even with power switched off, lethal voltages can exist in the equipment.

2. Open the computer and identify the empty slot in the card cage that is closest to the CPU. Do not leave any slots empty between the PMB-C and the CPU.

The PMB-C is a Universal PCI device and can be plugged into a slot which uses either 5V or 3.3V signaling protocol. Therefore, a J1 connector signaling key plug is not necessary.

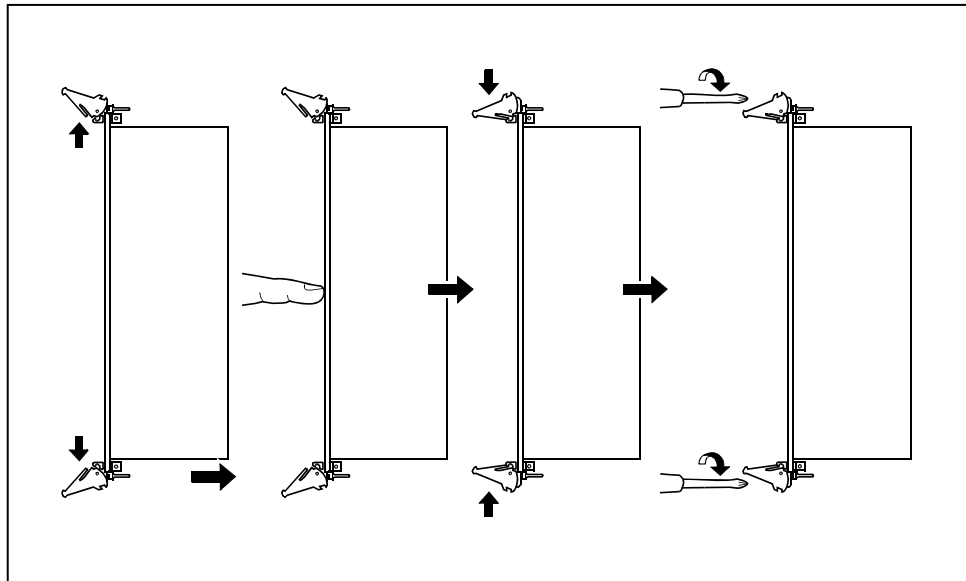
3. In the interest of allowing air flow, and if you have a choice, block off any unused slots in the cardcage so that fan air will not flow through them.

Caution

The static electricity that your body builds up normally can seriously damage the components on the computer boards.

4. Wear a grounded wrist strap. Touch a metal part of the computer chassis, remove the board from its anti static bag or container and immediately slide it into the slot.

Figure 2-2 Installing a CompactPCI Board



5. After making sure the board is seated correctly, lever the card in with the injector(s) and tighten the screwlock on each end of the faceplate.

Now, go to Section 2.6.

2.6 Finishing the Installation

There is no software to be installed that directly relates to the PMB-C. It is assumed that your operating system will already know how to deal with the 21154 PCI-PCI bridge chip. The bridge should actually be transparent to the software that operates with the PMC boards installed on the PMB-C.

This may sound a little like handwaving, but in fact, all major commercial operating systems have support for PCI-PCI bridges “wired” into the basic software because they are very commonly used to expand the PCI bus.

So, go ahead and install the software for your PMC modules that are on the PMB-C!

Hot Swap Support

Here *is* the handwaving: Some operating systems do have hot-swap support built in. For those that don't, you will need to write a driver to support it. Section 1.4 has some reference information for doing this, and Chapter 3 has some programming information for the 21154.

The following section has the hot swap procedure as documented by Sun.

2.7 Hotswap and Hotplug on a Solaris System

(Taken from is <http://docs.sun.com/source/806-6783-10/using.html#pgfId-29223>).

2.7.1 Introduction to Solaris Hot-swap and Hot-plug

You can initiate *hot-swapping* by pressing the card's ejector lever fully while the card is inserted; or by disengaging the ejector lever partially before the card is removed. You do not need to issue any commands to perform a hot swap. To perform a hot-plug operation, on the other hand, use the `cfgadm` command.

In order to hot-swap a CompactPCI (cPCI) card such as the PMB-C, you must boot the Solaris software in the domain where the cPCI card I/O assembly resides. When the Solaris software is booted in the domain, all cPCI cards are in the autoconfigure mode, and all configuring and unconfiguring can be performed without the `cfgadm` command.

When you insert a cPCI card using hot-swap, the card is automatically powered on and configured. When you remove a cPCI card using hot-swap, the card is automatically unconfigured and powered off.

See Sections 2.7.3 and 2.7.4 for *hot-swap* procedures.

Hot-plugging is accomplished by using the `cfgadm` command.

Note

You never need to issue any commands to perform a **hot swap**.

See Sections 2.7.5 for *hot-plug* procedures.

Note

Before you begin a *board-removal* procedure, make sure you have ready a board filler panel to replace the board you are going to remove from the system. A filler panel is a blank board with slots that allow cooling air to circulate

2.7.2 The *cfgadm* Command

The *cfgadm* command provides configuration administration operations on dynamically reconfigurable hardware resources. The following table lists the board states.

Table 2-1 Board States from the System Controller

Board States	Description
Available	The slot is not assigned to any particular domain.
Assigned	The board belongs to a domain, but the hardware has not been configured to use it. The board may be reassigned by the chassis port or released by the domain that it is assigned to.
Active	The board is being actively used by the domain to which it has been assigned. You cannot reassign an active board.

2.7.2.1 Displaying Basic Board Status

The *cfgadm* program displays information about boards and slots. Many operations require that you specify the system board names. To obtain these system names, at the #, type

#*cfgadm*

When used without options, *cfgadm* displays information about all known attachment points, including board slots and cPCI slots. The following display shows a typical output.

Table 2-2 Output of the Basic *cfgadm* Command

Ap_Id	Type	Receptacle	Occupant	Condition
N0.IB6	PCI_I/O_Boa	connected	configured	ok
N0.SB2	CPU_Board	connected	configured	ok
N0.SB3	unknown	empty	unconfigured	unknown
c0	scsi-bus	connected	configured	unknown

2.7.2.2 Displaying Detailed Board Status

For a more detailed status report, use the command

```
#cfgadm -av.
```

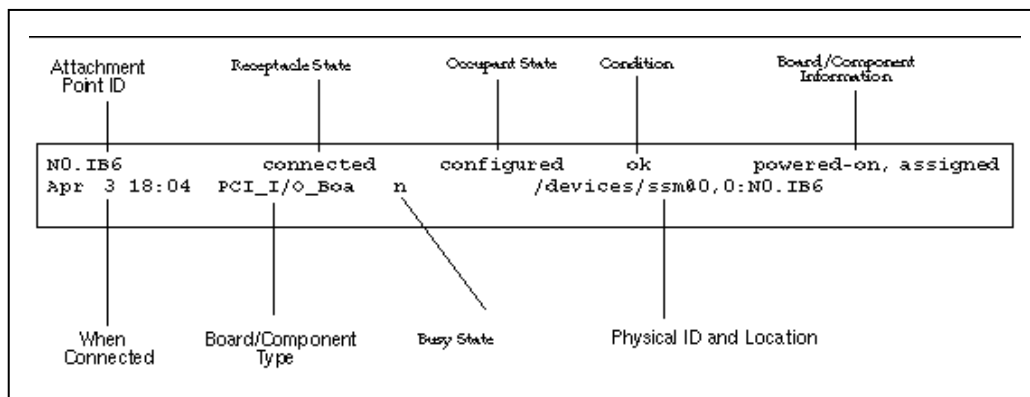
The -a option lists attachment points and the -v option turns on expanded (verbose) descriptions. The following table is a partial display produced by this command.

Table 2-3 Partial Output of the `cfgadm -av` Command

Ap_Id	Receptacle	Occupant	Condition	Information	When	Type	Busy	Phys_Id
N0.IB6	connected	configured	ok	powered-on, assigned	Apr 3 18:04	PCI_I/O_Boa	n	/devices/ssm@0,0:N0.IB6
N0.IB6::pci0	connected	configured	ok	device /ssm@0,0/pci @19,70000	Apr 3 18:04	io	n	/devices/ssm@0,0:N0.IB6::pci0
N0.IB6::pci1	connected	configured	ok	device /ssm@0,0/pci @19,60000	Apr 3 18:04	io	n	/devices/ssm@0,0:N0.IB6::pci1
N0.IB6::pci2	connected	configured	ok	device /ssm@0,0/pci @18,70000	Apr 3 18:04	io	n	/devices/ssm@0,0:N0.IB6::pci2
N0.IB6::pci3	connected	configured	ok	device /ssm@0,0/pci @18,60000	Apr 3 18:04	io	n	/devices/ssm@0,0:N0.IB6::pci3

[And so on. There will be a line for each PCI-mapped section for each board]

Table 2-4 Details of the Display for `cfgadm -av`



2.7.2.3 *cfgadm -c Command Options*

Table 2-5 *cfgadm -c Command Options*

<i>cfgadm -c</i> Option	Function
connect	The slot provides power to the board and begins monitoring the board. The slot is assigned if it was not previously assigned.
disconnect	The system stops monitoring the board and power to the slot is turned off.
configure	The operating system assigns functional roles to a board and loads device drivers for the board and for the devices attached to the board.
unconfigure	The system detaches a board logically from the operating system and takes the associated device drivers offline. Environmental monitoring continues, but any devices on the board are not available for system use.

2.7.2.4 *cfgadm -x Command Options*

Table 2-6 *cfgadm -x Command Options*

<i>cfgadm -x</i> Option	Function
assign	Adds (assigns) a board to a domain
unassign	Deletes (unassigns) a board from a domain
poweron	Powers on a system board
poweroff	Powers off a system board

2.7.3 Hot-swap - Insert the PMB-C

1. As superuser, identify the slot into which the PMB-C will be inserted.
2. Insert the PMB-C and push down on the ejector lever fully to engage it reliably. The card will be automatically powered-on and configured.
3. The blue Hotswap OK LED on the PMB-C should be off, the green Power LED on the I/O assembly should be lit, and the amber Hotplug OK LED on the I/O assembly should be off.

Note that insertion using hot-swap is equivalent to typing the following command:

```
#cfgadm -c configure ap_id.
```

where *ap_id* is the attachment point ID.

2.7.4 Hot-swap - Remove the PMB-C

Note

Before you hot-swap the PMB-C card, make sure that there is no I/O activity on that card.

1. Disengage the ejector lever slightly to deactivate the PMB-C.
2. Make sure the blue Hotswap OK LED on the PMB-C is lit, the amber Hotplug OK LED on the I/O assembly is lit, and the green Power LED on the I/O assembly is off.
3. Remove the PMB-C.
4. If the domain console is available, a message confirms that the PMB-C has been unconfigured.

2.7.5 Hot-Plug Removal and Replacement of the PMB-C

1. As superuser, identify the PMB-C card to be removed.

```
# cfgadm -s "select=class(pci)"
```

2. Detach (unconfigure) the PMB-C card to be removed:

```
# cfgadm -c unconfigure ap_id
```

where *ap_id* is the attachment point ID. The card is automatically unconfigured and powered-off.

3. Confirm that the card is detached.

```
# cfgadm -s "select=class(pci)" ap_id
```

4. When the green Power LED on the I/O assembly is off, the amber Hotplug OK LED on the I/O assembly is lit, and the blue Hotswap OK LED on the PMB-C card is lit, it is safe to remove the PMB-C.
5. After ensuring that you are properly grounded using a wrist strap, **remove and replace** the PMB-C.
6. After installing the PMB-C, attach (configure) it:

```
# cfgadm -c configure ap_id
```

When Solaris boots in a domain, all cPCI slots in that domain are in the autoconfigure mode by default. Hot-swap must be enabled for each slot.

1. To disable Autoconfiguration, use the following command:

```
# cfgadm -x disable_autoconfig ap_id
```

2. To re-enable Autoconfiguration, use the following command:

```
# cfgadm -x enable_autoconfig ap_id
```

The green Power LED on the I/O assembly will be lit and the blue Hotswap OK LED on the PMB-C should be off.

3. Verify that the card is attached.

```
# cfgadm -s "select=class(pci)" ap_id
```


Chapter 3

Programming On-board Devices

3.1 Introduction

This chapter covers the special programming features of the individual devices used on the PMB-C. It is intended to supply information unique to the board or to the application of a particular chip. Section 1.4 provides a list of appropriate publications that include manufacturer's data sheets and manuals.

Rastergraf does not provide software for the PMB-C at this time.

Registers in the 21154 PCI to PCI bridge control address mapping for the PMB-C. As part of the system initialization, system software (operating system and/or BIOS) generally set up the Base Address Registers (BARs) in the 21154 that enable access to its control registers, local PMC slots, and the Hot Swap control register.

If your OS or BIOS does not set up the 21154, a special device driver may be required to set up the 21154. Contact your OS vendor if this appears to be the case. Chapter 3 does have some information about the 21154 and you can get the data sheet and other technical information from the Intel web site. If you are totally stuck, please give Rastergraf a call and we will see what we can do to help you.

3.2 21154 Transparent PCI to PCI Bridge

Note

The *Intel Developer* has a lot of documentation for the 21154 available for download.

3.2.1 Introduction

The 21154BC Transparent PCI-to-PCI Bridge is currently used on the PMB-C. However, by 9/2002, the PMB-C will use the new and much more bug free FW21154BE.

The 21154 PCI-to-PCI bridge is designed for compliance with *PCI Local Bus Specification*, Revision 2.2. The 21154 has a 64-bit primary bus interface and a 64-bit secondary interface.

The 21154 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions. The 21154 has separate posted write, read data, and delayed transaction queues with significant buffering capability. In addition, the 21154 supports buffering of simultaneous, multiple, posted write and delayed transactions in both directions.

Among the features of the 21154 are: a programmable 2-level secondary bus arbiter, an IEEE standard 1149.1 JTAG interface, live insertion support, a 4-pin general-purpose I/O interface, individual secondary clock disables, and enhanced address decoding. Although not all used on the PMB-C, the 21154 has enough clock and arbitration pins to support nine PCI bus master devices directly on its secondary interface.

The 21154 allows the two PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation may increase system performance in applications such as multimedia.

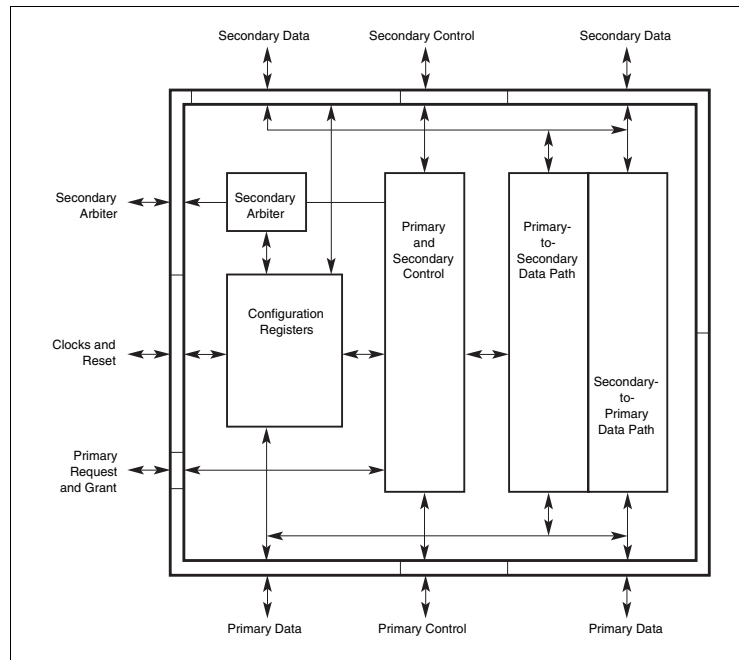
Features

- Designed for compliance with *PCI Local Bus Specification*, Revision 2.2
- Supports 64-bit extension signals on the primary and secondary interfaces

- Implements delayed transactions for all PCI configuration, I/O, and memory read commands – up to three transactions simultaneously in each direction
- Allows 152 bytes of buffering (data and address) for upstream posted memory write commands and 88 bytes of buffering for downstream posted memory write commands
- Allows 152 bytes of read data buffering upstream and 72 bytes of read data buffering downstream
- Provides concurrent primary and secondary bus operation to isolate traffic
- Provides ten secondary clock outputs:
 - Low skew, permitting direct drive of option slots
 - Individual clock disables, capable of automatic configuration during reset
- Provides arbitration support for nine secondary bus devices:
 - A programmable 2-level arbiter
 - Hardware disable control, permitting use of an external arbiter
- Provides a 4-pin general-purpose I/O interface, accessible through device-specific configuration space
- Provides enhanced address decoding:
 - A 32-bit I/O address range
 - A 32-bit memory-mapped I/O address range
 - A 64-bit prefetchable memory address range
 - ISA-aware mode for legacy support in the first 64 KB of I/O address range
- Includes live insertion support
- Provides VGA addressing and VGA palette snooping support
- Supports PCI transaction forwarding for the following commands:
 - All I/O and memory commands
 - Type 1 to Type 1 configuration commands
 - Type 1 to Type 0 configuration commands (downstream only)
 - All Type 1 to special cycle configuration commands
- Includes downstream lock support
- Supports both 5 V and 3.3 V signaling environments
- Provides an IEEE standard 1149.1 JTAG interface

3.2.2 Brief Functional Overview

Figure 3-1 21154 Block Diagram



Primary and Secondary Control

PCI interface control logic. This block contains state machines and control logic for the primary target interface, the primary master interface, the secondary target interface, and the secondary master interface. This block also contains logic that interfaces to the data path and the configuration block.

Primary-to-Secondary Data Path

Data path for data received on the primary interface and driven on the secondary interface. This block is used for write transactions initiated on the primary PCI bus and for returning read data for read transactions initiated on the secondary PCI bus. This block contains logic to store and, for posted write transactions, to increment the address of the current transaction. This block also performs bus command and configuration address format translations.

Secondary-to-Primary Data Path

Data path for data received on the secondary interface and driven on the primary interface. This block is used for write transactions initiated on the secondary PCI bus and for returning read data for read transactions initiated on the primary PCI bus. This block contains logic to store and, for posted write transactions, to increment the address of the current transaction. This block also performs bus command and configuration address format translations.

Configuration Registers

Configuration space registers and corresponding control logic. These registers are accessible from the primary interface only.

Secondary Bus Arbiter Control

Logic for secondary bus arbitration. This block receives `s_req_l<8:0>`, as well as the 21154 secondary bus request, and drives one of the `s_gnt_l<8:0>` lines or the 21154 secondary bus grant.

3.2.3 Use of the 21154 on the PMB-C

The 21154, is a transparent bridge, which allows both PMCs on the carrier to be visible to the system CPU. The wiring of the bridge to the PMC slots controls the mapping of PCI slot numbers to physical slots. PCI slots 0 and 1 are addressed at 0x8 and 0xd, respectively.

3.2.4 Interrupts

The PMB-C board follows the PCI Bridge Specification for interrupt address mapping which requires that the Interrupt Lines INTA#-INTD# be permuted. The interrupts are mapped as follows:

Table 3-1 Interrupt Mapping Between PMC and CompactPCI

CPCI	PMC Slot 0	PMC Slot 1
INTA	INTB	INTB
INTB	INTC	INTC
INTC	INTD	INTD
INTD	INTA	INTA

In addition, the PMC/CPCI INTx interrupt request lines for the slot that the PMB-C is itself plugged into may be permuted, which means that the boards INTx lines will be mapped to different interrupt lines depending on what slot it is plugged into. The device driver will usually notice this and compensate for it. In any case, because the permutations are all done in the backplane or PMB-C, the user has no direct control (e.g. jumpers) over any of this.

3.2.5 Bus Master Arbitration

The bridge implements the bus mastership control for the PMC slots. A two-level round-robin arbiter selects one master from among the slots 0 through 1 and the host PCI bus.

3.2.6 21154 Register Map

Table 3-2 21154 Register Map

31	16	15	00	
Device ID		Vendor ID		00h
Primary Status		Primary Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Primary Latency Timer	Cache Line Size	0Ch
Reserved				10h
Reserved				14h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status		I/O Limit Address	I/O Base Address	1Ch
Memory Limit Address		Memory Base Address		20h
Prefetchable Memory Limit Address		Prefetchable Memory Base Address		24h
Prefetchable Memory Base Address Upper 32 Bits				28h
Prefetchable Memory Limit Address Upper 32 Bits				2Ch
I/O Limit Address Upper 16 Bits		I/O Base Address Upper 16 Bits		30h
Reserved*			ECP Pointer*	34h
Reserved				38h
Bridge Control		Interrupt Pin	Reserved	3Ch
Arbiter Control		Diagnostic Control	Chip Control	40h
Reserved				44h-60h
gpio Input Data	gpio Output Enable Control	gpio Output Data	p_serr_I Event Disable	64h
Reserved	p_serr_I Status	Secondary Clock Control		68h
Reserved				6Ch-DBh
Power Management Capabilities**		Next Item Ptr**	Capability ID**	DCh
Data**	PPB Support Extensions**	Power Management CSR**		E0h
Reserved				E4h-FFh

3.2.7 21154 Device Identification

The table below lists the 21154 configuration registers which provide the device identification and revision. A complete description of all the 21154 registers is available by downloading the 21154 data sheet from the Intel web page.

Table 3-3 21154 Device ID Registers

Location	Value	Description
Vendor ID	0x1011	Intel, the manufacturer of the chip
Device ID	0x0026	21154-BC PCI to PCI Bridge chip
Revision	0x0005	21154-BC chip revision

3.3 CompactPCI Hot Swap

The PMB-C Hot Swap functionality is implemented using the “alternate register” method as defined in section 2.3.2.4 in the PICMG 2.1 R1.0 CompactPCI Hot Swap Specification. The 21154 PPB is not Hot Swap “silicon friendly”. That is, it does not have the Hot Swap Control and Status register as part of its configuration registers.

The CompactPCI Hot Swap Specification is designed to ensure that the PMB-C board may be removed and replaced in a live system without crashing it or damaging itself or other boards. The Specification includes the following additional features.

- **precharge** – using pull-ups on the PMB-C, PCI signal pins are brought to a 1 volt level prior to complete activation when “first power” is applied during insertion;
- **power sequencing** – applies power to the board’s components in a controlled manner;
- **control** - Hot Swap control and status register bits;
- **notification** – generates an interrupt whenever a Hot Swap event occurs;
- **information** – an LED mounted on the front panel indicate Hot Swap status to the user.

The Hot Swap mechanism depends both on system software and the CompactPCI connectors. Certain power and control pins are longer or shorter (staggered) so that as the board is inserted or extracted from the backplane the pins make early or late contact. This system implements mechanically-controlled power-sequencing so that the board can be powered on and off in a controlled manner.

Table 3-4 Hot Swap Power Sequencing

Connection Order	Backplane	PMB-C
First		First Power >>>
Main	Primary Power	>>>
	PCI Signals	>>>
	ENUM#	>>>
	HEALTHY#	>>>
Enabling	BD_SEL	>>>
	IDSEL	>>>

A General Purpose I/O (GPIO) register is located in the 21154's configuration registers. This register has 4 bits, each of which can be programmed as input or output.

Table 3-5 21154 GPIO Register As Used for Hot Swap

Name	Affects ENUM#	GPIO	Description
INS	yes	3	Indicates that the PMB-C has been inserted
EXT	yes	2	Indicates that the PMB-C is ready for extraction
LOO	no	1	Enable Blue LED on the PMB-C Front Panel
EIM	yes	0	Mask ENUM# - Disables Hot Swap System

It is known that Hot Swap is supported in Windows 2000 and XP, as well as Solaris 8. Other operating systems may also support it. Otherwise, as was mentioned before, special software will have to be developed for most proprietary systems.

An important point that has system implications is the need for the boards to be able to be reinitialized during normal operation. It has been customary in the past for PCI maps and initialization to occur during system startup and never again. Hot Swap requires that PCI enumeration and initialization become normal parts of the operating system day to day functions. This also, of course, means that all device drivers must be dynamically loadable, as a new option might be brought on line via a Hot Swap insertion.

Table 3-6 Complete Bit Map of 21154 GPIO Register

MSB								LSB								
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Bit
GPIO Input Data								GPIO Output Enable Control								Register
X	X	X	X	INS	EXT	X	X	X	X	X	X	l=out	l=out	l=out	l=out	Bits Definition

MSB								LSB								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit
GPIO Output Data								P_serr_1 Event Disable								Register
X	X	X	X	INS	EXT	LOO	EIM									Bits Definition

3.3.1 Full Hot Swap - Insertion

- 1) Before first inserting the PMB-C, follow the procedures in **Chapter 2** for mounting the PMC boards onto the PMB-C.
- 2) Initiate insertion by sliding the PMB-C into the selected CompactPCI slot. ESD strips on the edges of the board make contact with the card cage and discharge any accumulated electrostatic charges on the board to the cardcage through high-value resistors..
- 3) As the PMB-C makes contact with the Long Hot Swap pins in the backplane (see previous page), first power is applied to the 21154, which resets, then initializes and holds the PCI buses at high

impedance. The PMB-C Hot Swap circuit wakes up and lights the blue Hot Swap LED on the PMB-C front panel.

- 4) As the board is moved progressively into the backplane, the main power and PCI signals, which are on the standard length pins, now make contact.
- 5) Finally, when the board connects to the Short Hot Swap pins, BD_SEL# is asserted and IDSEL *can* be asserted. PMB-C (local) power control turns power on to the PMC boards. After a stabilizing period, PMB-C local reset is deasserted and the Hot Swap LED goes off.
- 6) Once the ejector handle next to the Hot Swap LED locks into place, a switch in the handle sets the INS bit. This asserts ENUM# on the CompactPCI bus, notifying system software that a Hot Swap event has occurred.
- 7) Because ENUM# is a bused signal, system software must poll all boards to determine who asserted ENUM#. The PMB-C can be identified by reading the Vendor and Device register (see Section 3.2.7)

3.3.2 Initializing the 21154 after a Hot Swap Insertion Event

Once the PMB-C has been identified as the board that generated the Hot Swap event, the 21154's GPIO registers should be initialized:

- 1) To make INS and EXT inputs and clear LOO and EIM, set byte 0x65 to 0xF and byte 0x66 to 0x3C.
- 2) A Hot Swap insertion event is identified by the INS bit (7) being set in byte 0x67.

To Clear the INS bit and deassert ENUM# from the CompactPCI, set byte 0x66 to 0x80 and then set byte 0x66 to 0x08.

- 3) The system software can now invoke the appropriate drivers and other software to activate the PMC board(s) on the PMB-C.

3.3.3 *ENUM# Mask and Hot Swap LED Control*

Once GPIO registers have been initialized as outlined in the previous sections, the EIM and LOO bits are controlled by byte 0x65.

- 1) To set LOO and light the blue Hot Swap LED, set byte 0x65 to 0x20.
- 2) To clear LOO and turn off the Hot Swap LED set byte 0x65 to 0x02.
- 3) To set EIM, which prevents ENUM# from being asserted on the CompactPCI bus, set byte 0x65 to 0x10.
- 4) To clear EIM, which allows ENUM# to be asserted on the CompactPCI bus, set the byte 0x65 to 0x01.

3.3.4 *Full Hot Swap - Extraction*

Important:

Prior to starting this phase, we assume that the 21154 bridge is either in the initial state after insertion or has been initialized by system software.

Use the following procedure to remove a board under Hot Swap control:

- 1) When the ejector handle next to the blue Hot Swap LED is pressed down to initiate extraction, the microswitch in the handle asserts EXT and ENUM#. **Board extraction should stop until the blue LED is lit.**
- 2) System software determines who asserted ENUM# by looking at each board in the system. A Hot Swap Extraction event is identified by the EXT bit (6) being set in byte 0x67.
- 3) To clear the EXT bit and deassert ENUM#, set byte 0x66 to 0x40 and then set byte 0x66 to 0x04.
- 4) Once the system software is prepared for complete board removal it lights the Hot Swap LED by setting byte 0x65 to 0x20.
- 5) When you see Hot Swap LED go on, you may completely remove the board from the machine.

Chapter 4

Troubleshooting

Introduction

This chapter contains information which should assist you in tracking down installation and functional problems with your board.

- 4.1 General procedures
- 4.2 Dealing with the PCI bus
- 4.3 Maintenance, Warranty, and Service

4.1 General Procedures

The PMB-C boards were designed with reliability and durability in mind. Nevertheless, it may happen that a problem will occur. This section is devoted to aiding the user in tracking down the problem efficiently and quickly.

You may be able to locate minor problems without technical assistance. If the problem can not be remedied, Rastergraf can then issue a Return Material Authorization (RMA) so that the board can be returned to the factory for quick repair.

It can happen that installing a new board will overload the computer's power supply if the power supply margins are exceeded. The first step in ascertaining if this is the problem is to calculate a power supply budget. This involves adding up the power requirements of each board in the system to see if you are within specification. Consult your computer's technical manual for information on how to correctly determine this. A typical PMB-C will draw a total of less than 1 Amp at +5 and +3.3 Volts.

When attempting to verify that the power supply is working properly, it is not unusual to unplug everything and measure the supply without a load. While this practice is acceptable for linear supplies, switching supplies (which are very commonly used in computers) require a certain load before proper regulation is achieved. Typically, at least 5 Amps must be drawn from the +5 Volt supply before the +12 volt supplies will give the proper readings.

4.2 Dealing with the PCI Bus

Because of the nature of the PCI protocol and the way support has been implemented in the Operating Systems for PCI bus devices such as the PMB-C, it is not possible to follow the same debugging strategies.

In fact, there are no address jumpers for these boards. Everything is configured in software through a set of on-board registers, which control the characteristics of the board as required by the PCI Specification.

The information used to program these registers is supplied to Operating System (OS) specific functions by Rastergraf's software. Ordinarily, several address map translations occur, including the CPU physical and virtual address maps and the CPU to PCI bridge address map.

While x86 systems generally follow the standards required to meet PC compatibility and mask these details, PowerPC systems do not. Among PowerPC vendors, there are no standards which ensure interoperability among CPU boards, even when they use the same CPU and PCI bridge.

Therefore, if you plan to use an PMB-C board in a PowerPC based system, it is vital to ensure that Rastergraf can vouch for the board's operation before you order the board. Otherwise, you may go crazy trying to figure out why it doesn't work. Please contact us at support@rastergraf.com or (541) 923-5530 if you have problems.

4.3 Maintenance, Warranty, and Service

Maintenance

The PMB-C requires no regular service, but if used in a particularly dirty environment, periodic cleaning with dry compressed air is recommended.

Because of the heat generated by normal operation of the board and other boards in the system, forced crossflow ventilation is required. If forced ventilation is not used IC temperatures can rise to 60 degrees C or higher. Such high temperature operation causes IC failures and reduced MTBF. With proper forced air cooling IC temperatures will be less than 35 degrees C.

Warranty

The PMB-C boards are warranted to be free from defects in material or manufacture for a period of 12 months from date of shipment from the factory. Rastergraf's obligation under this warranty is limited to replacing or repairing (at its option) any board which is returned to the factory within this warranty period and is found by Rastergraf to be defective in proper usage. This warranty does not apply to modules which have been subjected to mechanical abuse, electrical abuse, overheating, or other improper usage. This warranty is made in lieu of all other warranties expressed or implied. **All warranty repair work will be done at the Rastergraf factory.**

Return Policy

Before returning a module the customer must first request a Return Material Authorization (RMA) number from the factory. The RMA number must be enclosed with the module when it is packed for shipment. A written description of the trouble should also be included.

Customer should prepay shipping charges to the factory. Rastergraf will prepay return shipping charges to the customer. Repair work is normally done within ten working days from receipt of module.

Out of Warranty Service

Factory service is available for modules which are out of warranty or which have sustained damage making them ineligible for warranty repair. A flat fee will be charged for normal repairs and must be covered by a valid purchase order. If extensive repairs are required, Rastergraf will request authorization for an estimated time and materials charge. If replacement is required, additional authorization will be requested.

All repair work will be done at the Rastergraf factory in Redmond, Oregon, unless otherwise designated by Rastergraf.

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