

# RG-751

## VME Graphics Board User's Manual

**Rastergraf**

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Release 2.0

November 8, 2006

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## PREFACE

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This manual contains hardware and operating information for the RG-751 color graphics board. The standard configuration for the RG-751 includes 1 Mbyte of DRAM for instruction storage, 1Mbyte of underlay VRAM, 1/2 Mbyte of overlay VRAM an RS-232 serial interface for mouse or serial use, an AT keyboard interface, on-board AFGIS firmware, interface PAL set -PS25, and programmable video displayed in a 60Hz non-interlace format for use with VGA & SVGA video monitors. The RG-751 also has an optional interface for the Planar EL7768MS electroluminescent flat panel.

The RG-751 offers the following six programmable resolutions:

640h x 480v x 4  
640h x 480v x 8  
800h x 600v x 4  
800h x 600v x 8  
1024h x 768v x 4  
1024h x 768v x 8

The RG-751 is available in one basic configuration with the options listed below.

### Options

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To specify an option(s), add the option letter(s) to the basic part number. For example, RG-751-M4 would specify the basic configuration with 4 Mbytes of DRAM.

Option	Description	A24 Address	A32 Address
-PS25	Interface PAL Set	E00000h	E000 0000h
-PS26	Interface PAL Set	D00000h	D000 0000h
-PS27	Interface PAL Set	800000h	8000 0000h
-PS28	Interface PAL Set	A00000h	A000 0000h
-CP	Custom Interface PAL Set	xxxxxxh	xxxx xxxxxh
-50Hz	Specifies 50 Hz video timing		
-M4	Specifies 4 Mbytes of DRAM		
-EL1	Interface and Firmware for EL7768MS		
-BNC	Optional RGB BNC video connectors		

### Related Documents

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AFGIS Instruction Set Manual  
AFGIS Programming Manual  
AFGIS Assembler Manual  
AFGIS C Graphics Library Reference Manual  
AFGIS C Programming Manual  
AFGIS Application Interface Manual  
TMS34010 User's Guide (available from Texas Instruments)

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## WARRANTY

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3. Damage results from connecting the hardware to incompatible equipment.

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# 1.0 INTRODUCTION

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## Chapter Contents:

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### **The RG-751 Color Graphics Board**

#### **1.1 Overview**

#### **1.2 Features**

##### **1.2.1 Software Support**

##### **1.2.2 Video Monitor Support**

#### **1.3 Typical System Usage**

#### **1.4 Manual Organization**

## The RG-751 Color Graphics Board

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### 1.1 Overview

The RG-751 is a high performance 6U graphics board, powered by the TMS34010 graphics processor, and designed for VMEbus applications. Major features of the RG-751 are its on-board AFGIS firmware with over 250 highly optimized graphics primitives for easy graphics programming; its ability to support real-time multi-tasking operating systems with its unique pointer based graphics environment; its advanced hardware architecture with overlay and underlay display pages; and extensive C programming support.

The RG-751 is ideal for simple embedded system applications, because it is easy to program and because it does its own local graphics processing, freeing the VMEbus host to do other things while the RG-751 is creating graphics in parallel.

The real power and versatility of the RG-751 is evident when it is used with real-time multi-tasking operating systems that require several tasks to independently generate graphics on the video screen. Each task can have its own colors, font, screen position, etc., and can independently create graphics on the video screen without affecting the colors, font, screen position, etc. of any other task.

Each task can have its own private pointer based graphics environment with all the necessary buffers, variables, and low level drawing parameters. The host processor (typically the driver) selects the environment for the current task by updating a pointer in Fixed RAM before the task runs any graphics code. Because the graphics environment is pointer based, switching the environment takes little time, typically less than 15 usecs, which has a minimal impact on the task's allocated time slice.

The RG-751 is supported with the AFGIS C Graphics Library which has over 125 high level C functions which have been optimized for use with the on-board AFGIS firmware. A driver is typically required for use with the AFGIS C Graphics Library and today's modern real-time operating systems. Drivers are available for several of the popular real-time operating systems, and custom driver development is available from Rastergraf, Inc. for operating systems not currently supported with drivers.

The driver and AFGIS C Graphics Library are easy to install, and once installed, allow the user to begin using the RG-751 without regard for the details of the hardware interface, as these are handled by the driver. The C functions provided by the AFGIS C Graphics Library are linked at compile time, and in effect extend the C functions of the system's C compiler to include those provided by the AFGIS C Graphics Library.

The combination of advanced hardware architecture with overlay and underlay planes, its optimized on-board graphics primitives, and its extensive C programming support, make the RG-751 an ideal low cost, high performance graphics board for today's medical and industrial applications.

## The RG-751 Color Graphics Board

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### 1.2 Features

The RG-751 provides the following major features and options:

- Programmable Resolutions
  - 640h x 480v x 4/8
  - 800h x 600v x 4/8
  - 1024h x 768v x 4/8
- 16/256 Colors
- TMS34010 Graphics Processor
- Use with VGA or SVGA monitors
- 1 Mbyte of DRAM (option for 4 Mbytes)
- 2 Pages of VRAM
  - Overlay Page with 16 colors
  - Underlay Page with 256 colors and hardware pan and zoom
- Mouse and Keyboard Interfaces
- Supports parallel processing for improved system performance
- Interrupts to and from the VMEbus
- On-board firmware with over 250 highly optimized graphics primitives to draw text, windows, circles, arcs, polygons, fills, fatlines, pattern fills and more!
- AFGIS C Graphics Library for easy graphics programming
- Supports Real-Time Multi-Tasking Operating Systems
- Fast graphics environment switching, less than 15 usec to support real-time tasks
- Drivers for VMEexec, VxWorks, OS-9, PSOS, VRTXsa, LynxOS, and PDOS real-time operating systems
- Application interface to extend the on-board graphics primitives with downloaded TMS34010 code.
- Flicker Free 60 Hz non-interlaced display format

### 1.2.1 Software Support

Software support for the RG-751 graphics board includes development tools that run under DOS or OS-9® operating systems. Included are the AFGIS Assembler, AFGIS C Graphics Libraries, and software development tools. RAVE® and X Windows® are supported for OS-9 applications using the Motorola 147 and 167 processors. In the OS-9 environment, the software development tools can be used to develop graphics code directly on an RG-751 installed in a VMEbus system. In the AT environment, these tools can be used with an AT computer to develop AFGIS assembly code that can be downloaded to an RG-751 via the serial port. The code can be executed in the AT environment by installing an RG-91x graphics board in an AT computer. Interface code written in C is available to assist in the development of custom drivers.

### 1.2.2 Video Monitor Support

The RG-751 Color Graphics Boards output an RS-343 composite video signal in a flicker-free 60 Hz non-interlaced format. The RG-751 video outputs are compatible with Multisync™ monitors, VGA monitors, conventional RGB color monitors accepting analog inputs, and monochrome monitors (see the *Installation* chapter for more information). The Planar® EL640.350-D Series and EL7768MS VGA electroluminescent displays are also supported by the RG-751 board. Custom monitor interface requirements can usually be supported by modifying the video timing parameters and changing the pixel clock frequency.

## 1.3 Typical System Usage

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The basic operation of the RG-751 board in a VMEbus system is as follows:

- The user locates the RG-751 board in VMEbus address space using jumper J3.
- The RG-751 memory mapped registers and RAM are initialized at power up by the AFGIS firmware.
- The RG-751 board interface registers are configured at power up by the VMEbus CPU. AFGIS instructions are loaded into RG-751 memory by the VMEbus CPU.
- The AFGIS instructions are executed by RG-751, producing graphic images on the video monitor connected to the RG-751 board.
- The RG-751 board has eight connectors for external peripherals. A high resolution monitor can be connected to three BNC connectors (J10/J11/J12) or to DB15F connector J13. An electroluminescent display can be connected to J7 (a 2x8 pin header) and to J6 (a 2x13 pin header). J15 is a DB9F connector for the serial mouse/RS-232 serial port. J14 is a DB9F connector for the AT keyboard interface

## 1.4 Manual Organization

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### Chapter Summaries

The following chapters describe the operation and design of the RG-751 graphics board.

**2.0 Installation** contains RG-751 jumper and connector information.

**3.0 Operation** provides an overview of RG-751 board operation. The reader is referred to additional sections of this chapter for detailed information on specific elements of board operation. Registers and Memory Maps provide reference material such as memory maps and register descriptions. Serial Port includes serial port configuration, serial mouse interface, and UART register information. AT Keyboard Port describes the AT keyboard interface on the RG-751 board.

**4.0 Specifications** includes power requirements and video timing specifications.

**Appendix A** Interface PAL Equations

**Appendix B** VME CPU to RG-751 Data Transfer

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## 2.0 INSTALLATION

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#### 2.2 Board Layout

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2.3.2 J2 Run/Halt at Power-up

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2.3.4 J4 Resolution Select/Configuration

2.3.5 J5 Clock Select

2.3.6 J8 RS-232 TxD/RxD

2.3.7 J9 RS-232 RTS/CTS

#### 2.4 LEDs

#### 2.5 Connectors

2.5.1 Planar® EL7768MS Electroluminescent  
Display Connector

2.5.2 DB15 Video Connector

2.5.3 AT Keyboard Connector

2.5.4 RS-232 Serial Connector

2.5.5 VMEbus Connector

## 2.1 Board Installation

Install the RG-751 board in a VMEbus card slot. The RG-751 must plug into VMEbus connectors P1 and P2.

**CAUTION!**

Switch off power to the VMEbus before installing the RG-751 to avoid possible damage to the graphics board or host hardware.

## 2.2 Board Layout

The RG-751 graphics board contains several jumper options, connectors and status LEDs, as shown in Figure 2.1. Connectors are provided for interfacing the RG-751 to a video monitor (J13), Planar® electroluminescent display (J6 and J7), keyboard (J14), and serial device (J15).

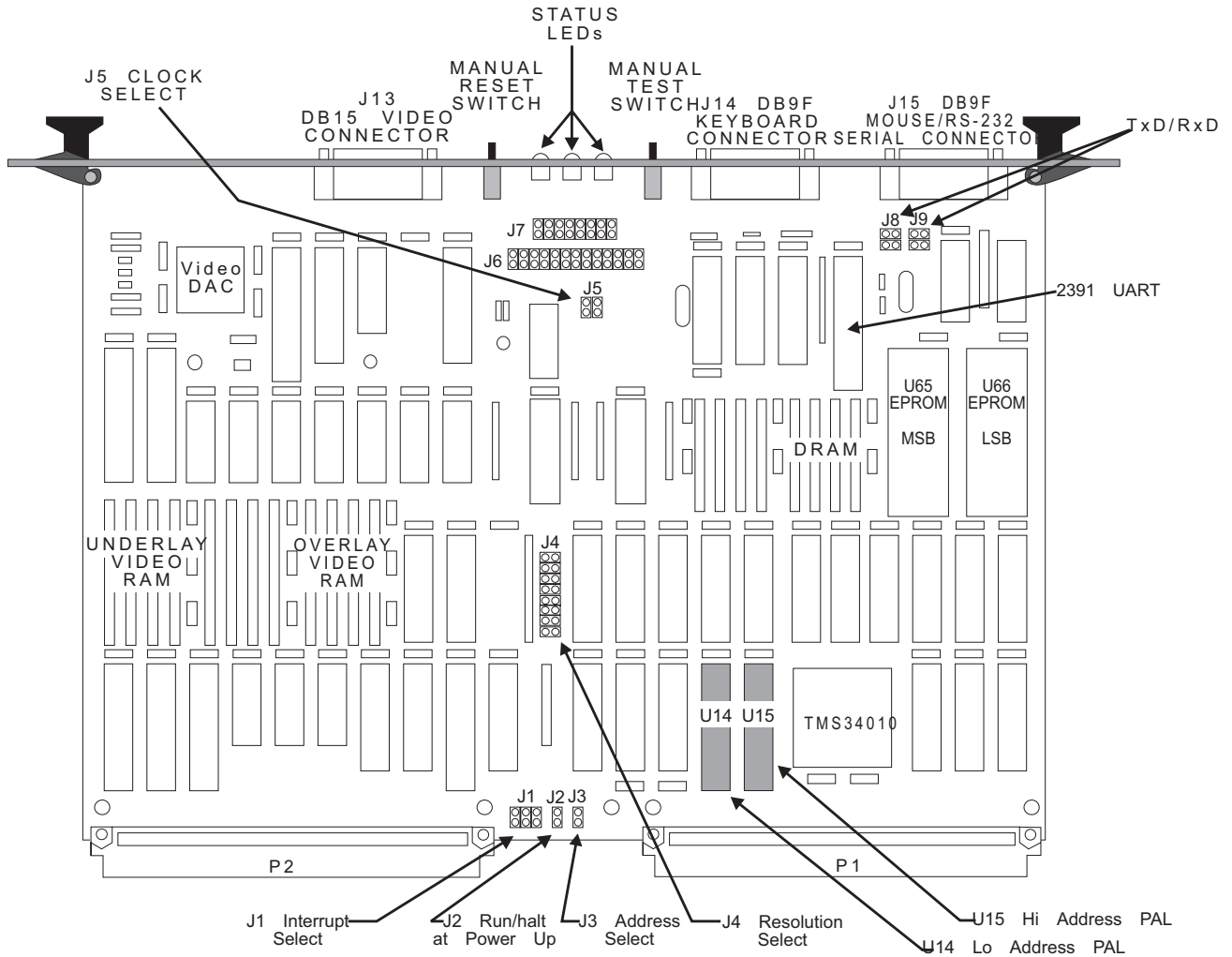


Figure 2.1 RG-751 Board Layout

### 2.3 Jumper Options

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The following jumper options, as shown in Figure 2.2, are available on the RG-751. Figure 2.1 indicates the jumper locations. Use shorting clips or wirewrap wire to select the jumper options.

JUMPER	DESCRIPTION
J1	Interrupt Request Select
J2	Run/Halt at Power-up
J3	A24/A32 Address Select
J4	Resolution Select/Configuration
J5	Clock Select
J6	Video Connector for Planar® EL7768MS Electroluminescent VGA Display (26 pin header)
J7	Video Connector for Planar® EL7768MS Series Electroluminescent Display (16 pin header)
J8	RS-232 TxD/RxD Swap
J9	RS-232 CTS/RTS Swap

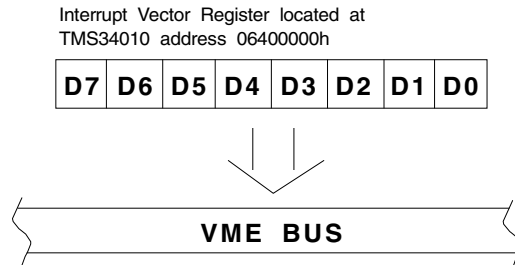
**Figure 2.2 Jumper Summary**

**2.3 Jumper Options (continued)**

**2.3.1 J1 Interrupt Request Select**

The RG-751 generates an interrupt to the host and outputs an 8 bit interrupt vector in response to an interrupt acknowledge, as shown in Figure 2.3a. The interrupt can be routed to any of the 7 VMEbus interrupt lines, IRQ1-IRQ7, by installing jumpers in J1 as shown below in Figure 2.3.

IRQ	J1	J1																
		<table border="1"> <tr> <td></td> <td>2</td> <td>4</td> <td>6</td> </tr> <tr> <td>□</td> <td>□</td> <td>□</td> <td>□</td> </tr> <tr> <td>□</td> <td>□</td> <td>□</td> <td>□</td> </tr> <tr> <td>1</td> <td>3</td> <td>5</td> <td></td> </tr> </table>		2	4	6	□	□	□	□	□	□	□	□	1	3	5	
	2	4	6															
□	□	□	□															
□	□	□	□															
1	3	5																
IRQ1	J1	5-6																
IRQ2	J1	3-4																
IRQ3	J1	3-4, 5-6																
IRQ4	J1	1-2																
IRQ5	J1	1-2, 5-6																
IRQ6	J1	1-2, 3-4																
IRQ7	J1	1-2, 3-4, 5-6																



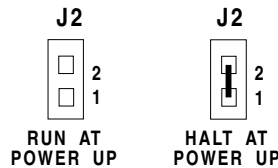
**Figure 2.3a Interrupt Vector Register**

**Figure 2.3 IRQ Select**

**2.3 Jumper Options (continued)**

**2.3.2 J2 Run/Halt at Power-up**

The RG-751 can be jumpered at J2 to come up running (no jumper at J2) or halted (jumper installed in J2) at power-up. For normal operation, the RG-751 should be jumpered to come up running.

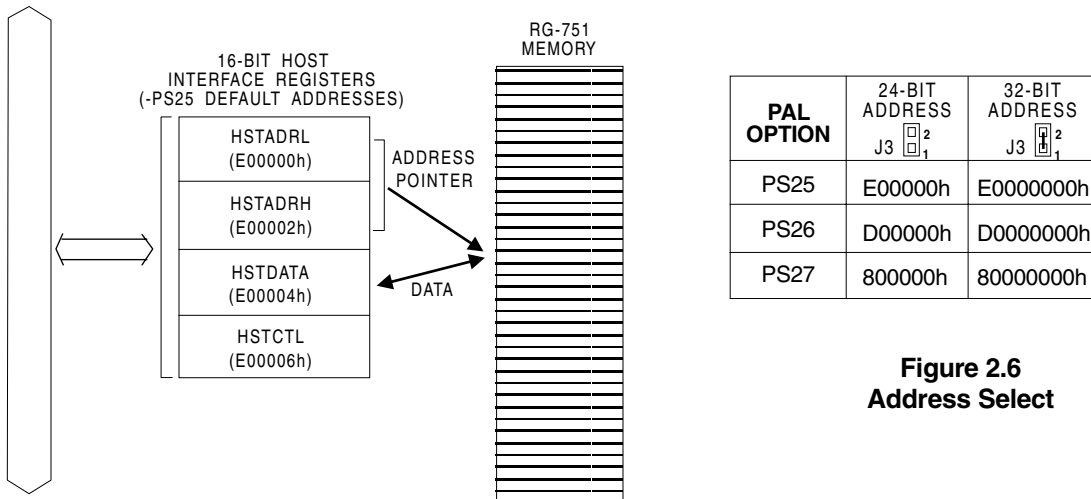


**Figure 2.4 Run/Halt at Power-Up Jumper**

**2.3.3 J3 A24/A32 Address Select**

The VMEbus interfaces to the RG-751 via four 16-bit Host Interface Registers located in a 256-byte page in VMEbus memory space (see Figure 2.5). All data transfers between the VMEbus and the RG-751 are via these registers. The four 16-bit Host Interface Registers can be located in 24-bit or 32-bit VMEbus address space by configuring jumper J3 (see Figure 2.6). With a jumper installed in J3, a 32-bit address is selected. With no jumper installed in J3, a 24-bit address is selected.

The base addresses are determined by the Interface Register PALs U14 and U15, and can be changed by programing a new PAL set (see Appendix A for PAL equations) or by ordering a custom Interface PAL set from Rastergraf.



**Figure 2.6 Address Select**

**Figure 2.5 VMEbus Interface**

2.3 Jumper Options (continued)

2.3.4 J4 Resolution Select/Configuration

Jumper J4:1-2, 3-4, 5-6, and 7-8 are used to select the graphics board resolution (see Figure 2.7). The remaining jumpers of J4 are used for other options as shown in Figures 2.8 and 2.9.

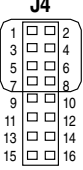

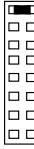
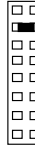
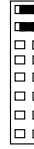

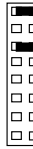
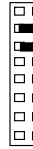
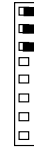





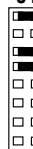
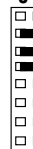

								
<b>RESOLUTION</b>	640h x 480v x 4	640h x 480v x 8	800h x 600v x 4	800h x 600v x 8	1024h x 768v x 4	1024h x 768v x 8		
								
	EL7768MS 640h x 480v x 4							

Figure 2.7 Resolution Jumper Select

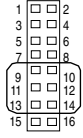




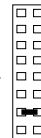

<b>FUNCTION</b>	
<b>SYNC ON GREEN</b> 9-10	  DISABLED    ENABLED
<b>H SYNC POLARITY</b> 11-12	  POSITIVE    NEGATIVE
<b>V SYNC POLARITY</b> 13-14	  POSITIVE    NEGATIVE

Figure 2.8 Function Select

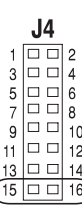


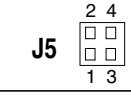
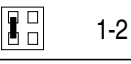
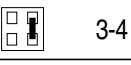
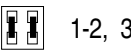
		
	DEBUG DISABLED	DEBUG ENABLED

Figure 2.9 Debug Enable

**2.3 Jumper Options (continued)**

**2.3.5 J5 Clock Select**

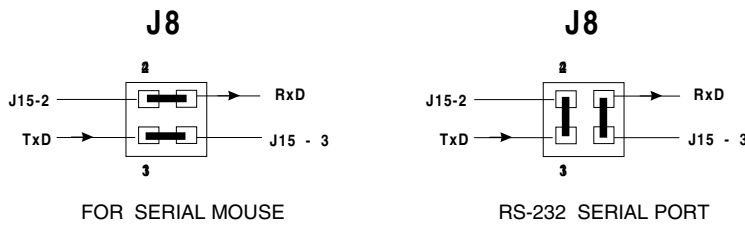
This jumper is used to select the clock for the TMS34010 graphics processor (see Figure 2.10).

TMS34010 CLOCK	J5	
not used	J5	
40.00 MHz	J5	 <span style="margin-left: 20px;">1-2</span>
not used	J5	 <span style="margin-left: 20px;">3-4</span>
not used	J5	 <span style="margin-left: 20px;">1-2, 3-4</span>

**Figure 2.10 Clock Select Jumper**

**2.3.6 J8 RS-232 Transmit/Receive (TxD/RxD)**

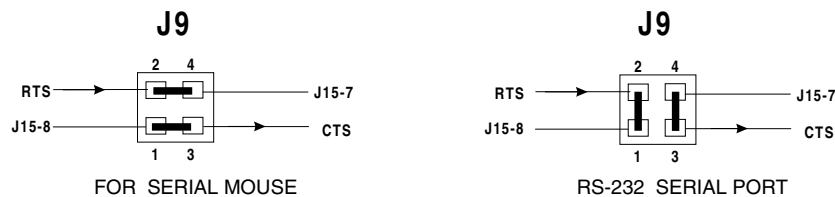
RS-232 transmit (TxD) and receive data (RxD) can be swapped by installing a jumper in J8, as shown in Figure 2.11.



**Figure 2.11 RS-232 TxD and RxD Data Lines**

**2.3.7 J9 RS-232 Handshake (RTS/CTS)**

Two RS-232 handshake signals, RTS and CTS can be swapped by installing jumpers in J9 as shown in Figure 2.12.



**Figure 2.12 RS-232 RTS and CTS Handshake Lines**

**2.4 LEDs**

Three LEDs on the RG-751 provide status information (see Figure 2.1).

**Red LED:**

The red LED lights when an error is detected. The red LED can be user programed with the LED opcode.

**Yellow LED:**

The yellow LED lights when the board is accessed by the bus.

**Green LED:**

The green LED blinks when the TMS34010 is in the idle loop. The green LED can be user programed with the LED opcode.

**2.5 Connectors**

The RG-751 board has connectors for VMEbus, VGA/SVGA video monitor, an AT keyboard, a serial port, and a Planar EL7768MS EL Flat Panel display (see Figure 2.13). Connector signals and cabling requirements are described in the following pages.

REFERENCE NUMBER	DESCRIPTION	TYPE
P1	VMEbus connector	96-pin connector
P2	VMEbus connector	96-pin connector
J6	Planar® EL7768MS Electroluminescent VGA Display	2x13 pin header
J7	Planar®EL7768MS Electroluminescent VGA Display	2x8 pin header
J10	Video connector -Blue (optional)	BNC
J11	Video connector -Green (optional)	BNC
J12	Video connector -Red (optional)	BNC
J13	Video connector	DB15F
J14	AT keyboard connector	DB9F
J15	Serial/mouse connector	DB9F

**Figure 2.13 Connector References**

2.5 Connectors (continued)

2.5.1 J6-J7 Planar® EL7768MS Electroluminescent VGA Display Connector

A Planar EL7768MS electroluminescent flat panel display can be connected to the RG-751 with two flat ribbon cables as shown in Figures 2.14 and 2.15.

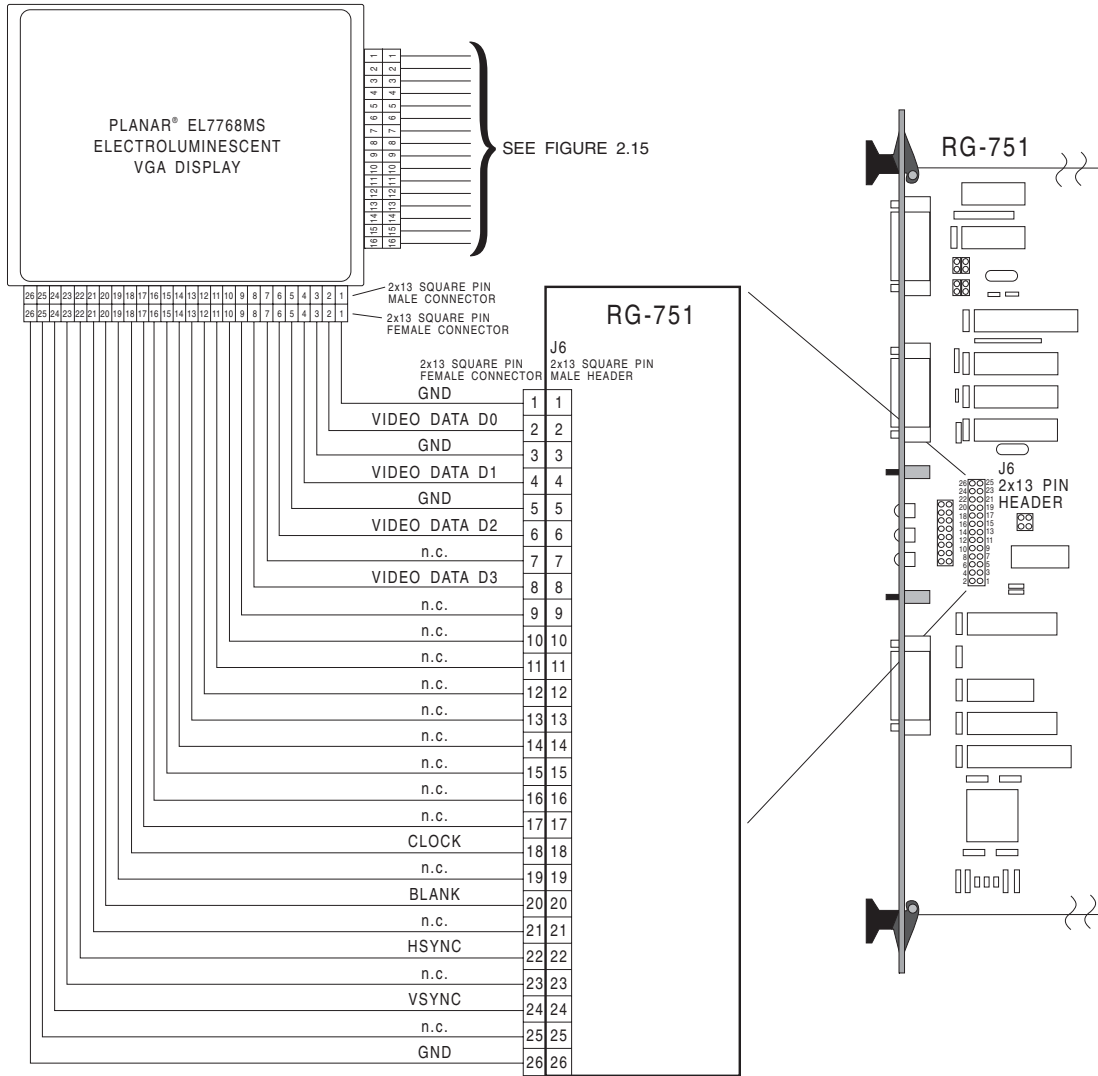


Figure 2.14 26 Pin Connection To Planar EI7768MS Display

2.5 Connectors (continued)

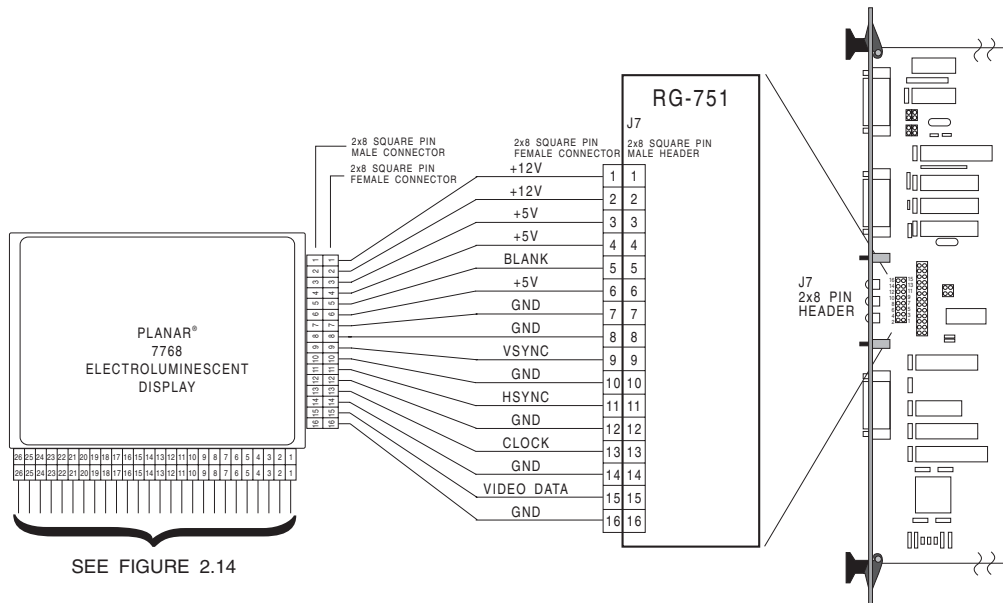


Figure 2.15 16 Pin Connection To Planar EI7768MS Display

2.5 Connectors (continued)

2.5.2 J10-J13 Video Output Connectors

A VGA or SVGA video monitor can be connected to the RG-751 DB15F connector J13 (see Figure 2.16) or to the optional BNC connectors J12 (red), J11 (green), and J10 (blue), as shown in Figure 2.17.

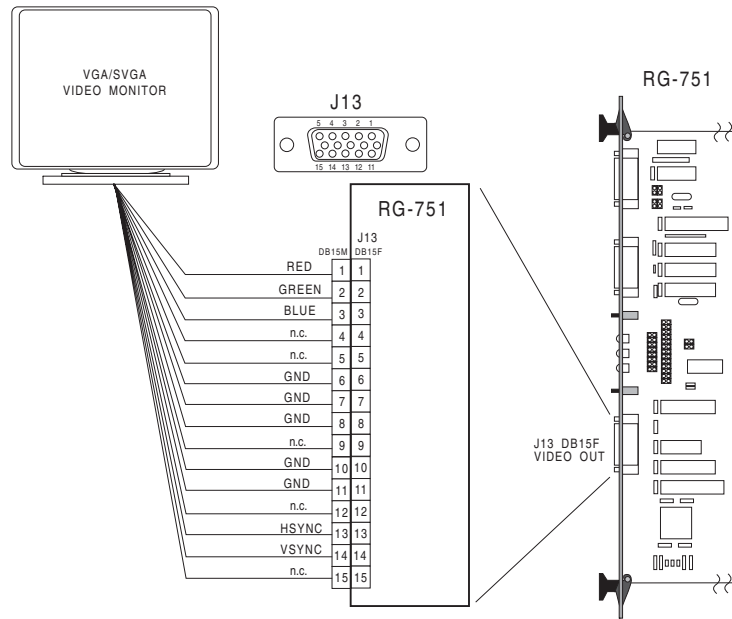


Figure 2.16 DB15 Connection To Video Monitor

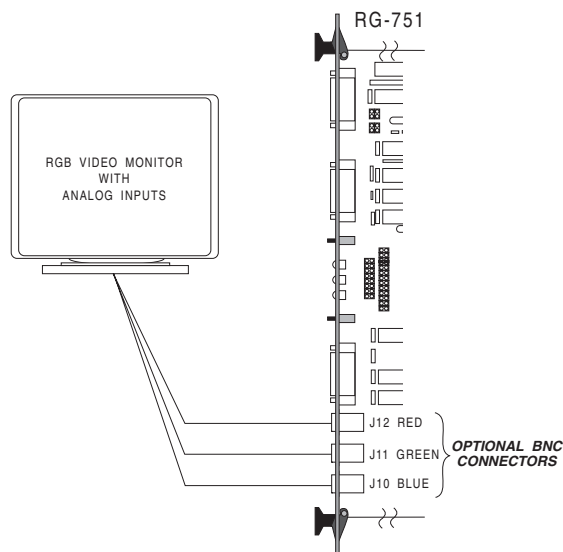


Figure 2.17 Optional BNC Connection To Video Monitor

2.5 Connectors (continued)

2.5.3 J14 AT Keyboard Connector

Connector J14 provides an interface to a standard AT keyboard. An adapter cable is required to connect the standard AT 5-pin keyboard connector to the RG-751 board DB9 connector (see Figure 2.18). The RG-751 keyboard firmware works with an AT style keyboard - it does not operate with PC or XT keyboards, which have a different interface.

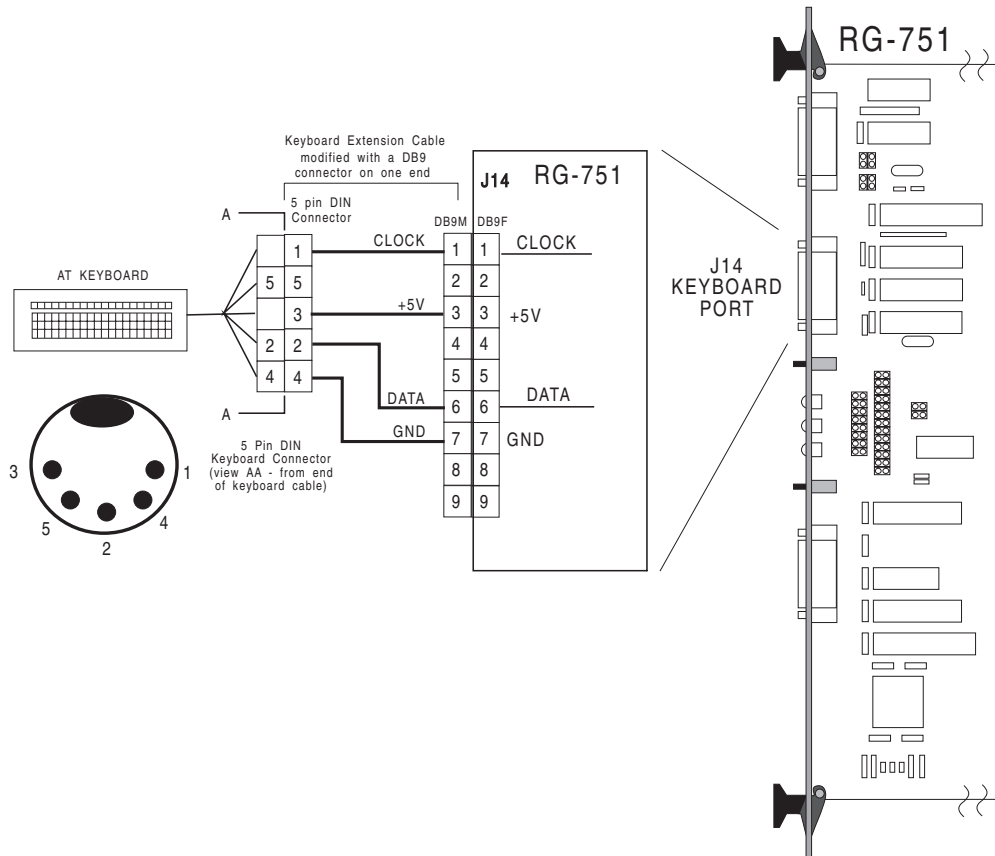


Figure 2.18 AT Keyboard Connection To J14

2.5 Connectors (continued)

2.5.4 J15 RS-232 Serial Connector

RS-232 connector J15 can be configured for serial data transfer or for use with a serial mouse by configuring the jumpers at J8 & J9, as shown in Figures 2.19 & 2.20.

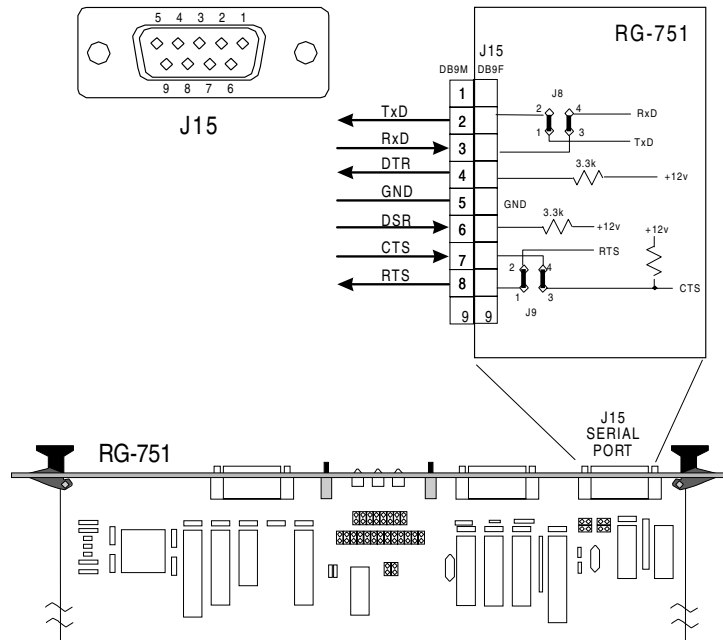


Figure 2.19 RS-232 Serial Data Configuration

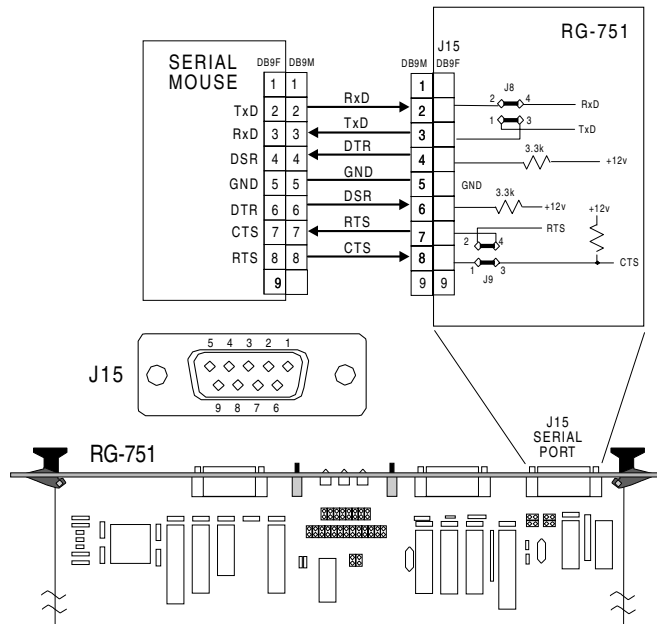


Figure 2.20 Serial Mouse Configuration

**2.5 Connectors (continued)**

**2.5.5 VMEbus Pin Assignments**

Figure 2.21 shows the VMEbus P1 and P2 connector pin assignments used by the RG-751 graphics board.

P1				P2			
PIN #	ROW A	ROW B	ROW C	PIN #	ROW A	ROW B	ROW C
1	D0	D8	1				
2	D1	D9	2				
3	D2	BG0IN*	D10	3			
4	D4	BG0OUT*	D11	4	A24		
5	D4	BG1IN*	D12	5	A25		
6	D5	BG1OUT*	D13	6	A26		
7	D6	BG2IN*	D14	7	A27		
8	D7	BG2OUT*	D15	8	A28		
9	BG3IN*	9	A29				
10	BG3OUT*	10	A30				
11	11	A31					
12	DS1*	12					
13	DS0*	LWORD*	13				
14	WRITE*	AM5	14	D16			
15	A23	15	D17				
16	DTACK*	AM0	A22	16	D18		
17	AM1	A21	17	D19			
18	AS*	AM2	A20	18	D20		
19	AM3	A19	19	D21			
20	IACK*	A18	20	D22			
21	IACKIN*	A17	21	D23			
22	IACKOUT*	A16	22				
23	AM4	A15	23	D24			
24	A7	IRQ7*	A14	24	D25		
25	A6	IRQ6*	A13	25	D26		
26	A5	IRQ5*	A12	26	D27		
27	A4	IRQ4*	A11	27	D28		
28	A3	IRQ3*	A10	28	D29		
29	A2	IRQ2*	A9	29	D30		
30	A1	IRQ1*	A8	30	D31		
31	-12 VDC	+12 VDC	31				
32	+5 VDC	32					

**Figure 2.21 VMEbus Connectors P1 & P2 Pin Assignments**



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## 3.0 OPERATION

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### Chapter Contents:

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- 3.1 Overview of RG-751 Operations**
  - 3.1.1 Power Up Display**
  - 3.1.2 Operation Overview**
- 3.2 RG-751 Host Interface Registers**
  - 3.2.1 Data Transfer Conversion**
  - 3.2.2 Transferring Data**
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  - 3.3.1 RG-751 Memory Map**
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  - 3.3.6 Remapping DRAM with ROMDIS**
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- 3.6 Interrupts to the VMEbus from RG-751**
- 3.7 Coordinate System**

### 3.1 Overview of RG-751 Operation

#### 3.1.1 Power Up Display

The RG-751 creates a display at power up, indicating the resolution of the current display mode. The display resolution is programmable, and can be changed with the CONFIG opcode. The parameter following the CONFIG opcode changes the resolution as follows:

<u>CONFIG</u>	<u>PARAMETER</u>	<u>RESOLUTION</u>
0021	0000	= 640h x 480v x 4
0021	0001	= 640h x 480v x 8
0021	0002	= 800h x 600v x 4
0021	0003	= 800h x 600v x 8
0021	0004	= 1024h x 768v x 4
0021	0005	= 1024h x 768v x 8

The default resolution is 640h x 480v x 4.

#### 3.1.2 Operation Overview

When programing the RG-751 using an RGI driver and AFGIS C graphics library, the details of loading and executing instructions are transparent to the user, as the driver interfaces to both the operating system and the RG-751. The user merely calls the specified C graphics functions from the AFGIS C graphics library, and the resulting code is passed to the driver, which interfaces appropriately with the RG-751.

However, the RG-751 can be programed directly with AFGIS opcodes. AFGIS opcodes are 16 bit instructions which may have 16 bit parameters, similar to most assembly languages. AFGIS opcodes are executed by the on-board firmware after they have been loaded into RG-751 memory. The default location for loading AFGIS opcodes is 03100000h. Execution of these opcodes begins when the host issues a HINT0 interrupt to the RG-751. The list of AFGIS opcodes (display list) must end with the EODL opcode, which causes display execution to cease when the EODL opcode is processed. When the EODL instruction has been executed by the RG-751, AFGIS firmware will issue an interrupt to the VMEbus or set the EODLFLAG, indicating to the host that display execution has been completed.

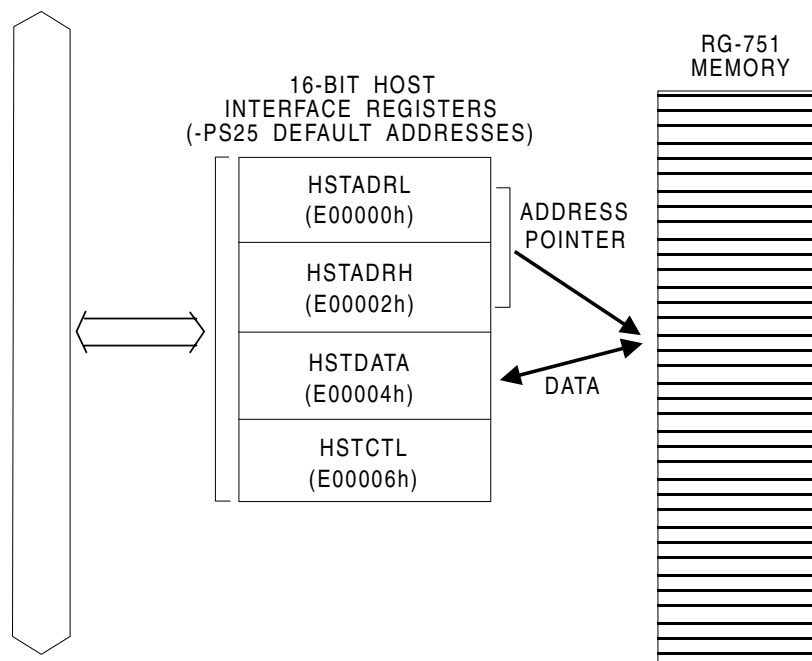
HINT0 causes execution to begin at the address in Fixed RAM location HINT0\_AFG\_ENTRY. The default value in HINT0\_AFG\_ENTRY is 03100000h, but can be changed by the host to any valid TMS340x0 address, and display execution will begin at the specified address in response to HINT0. HINT0\_AFG\_ENTRY is located in Fixed RAM at 030000C0h.

See the AFGIS Programing Manual for more information.

### 3.2 RG-751 Host Interface Registers

The VMEbus interfaces to the RG-751 via four 16-bit Host Interface Registers located in a 256-byte page in VMEbus address space. All data transfers between the VMEbus and the RG-751 are via these registers, and data must be transferred 16 bits at a time. The four

16-bit Host Interface Registers can be located at one of two base addresses by configuring jumper J3. The two base addresses are determined by the Interface Register PALs U14 and U15, and can be changed by programming new PALs (see Appendix A for PAL equations) or by ordering a custom Interface PAL set from Rastergraf, Inc.



**Figure 3.1 Host Interface Registers**

#### 3.2.1 Data Transfer Conventions

The RG-751 supports little endian format. Words, 16 bit values, can be transferred from VMEbus memory to RG-751 memory across the VMEbus without modification. Bytes (8 bit values) must be byte swapped and longs (32 bit values) must be word swapped before transfer. See Appendix B for more information.

### 3.2 RG-751 Host Interface Registers (continued)

#### 3.2.2 Transferring Data

Data is transmitted to or from the RG-751 by specifying the TMS34010 32-bit memory address in HSTADRL and HSTADRH, and then by writing or reading a 16-bit data word to or from the HSTDATA register. The TMS34010 moves the data from RG-751 memory to the HSTDATA register for a read operation, or from the HSTDATA register to the specified memory location on the RG-751 graphics board for a write operation. The TMS34010 is a bit-addressable machine. AFGIS opcodes must be loaded on word boundaries (the four lsbs of the address loaded into HSTADRL must be zero). Bits in the HSTCTL register can be set to cause the address value in HSTADRL/H to increment automatically on reads or writes, to pass interrupts to the RG-751, and to control the TMS34010 graphics processor. See the TMS34010 User's Guide available from Texas Instruments for a complete description of the TMS34010 host interface.

#### HSTADRL

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
-----	-----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	----

#### HSTADRH

A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----

#### HSTDATA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-----	-----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	----

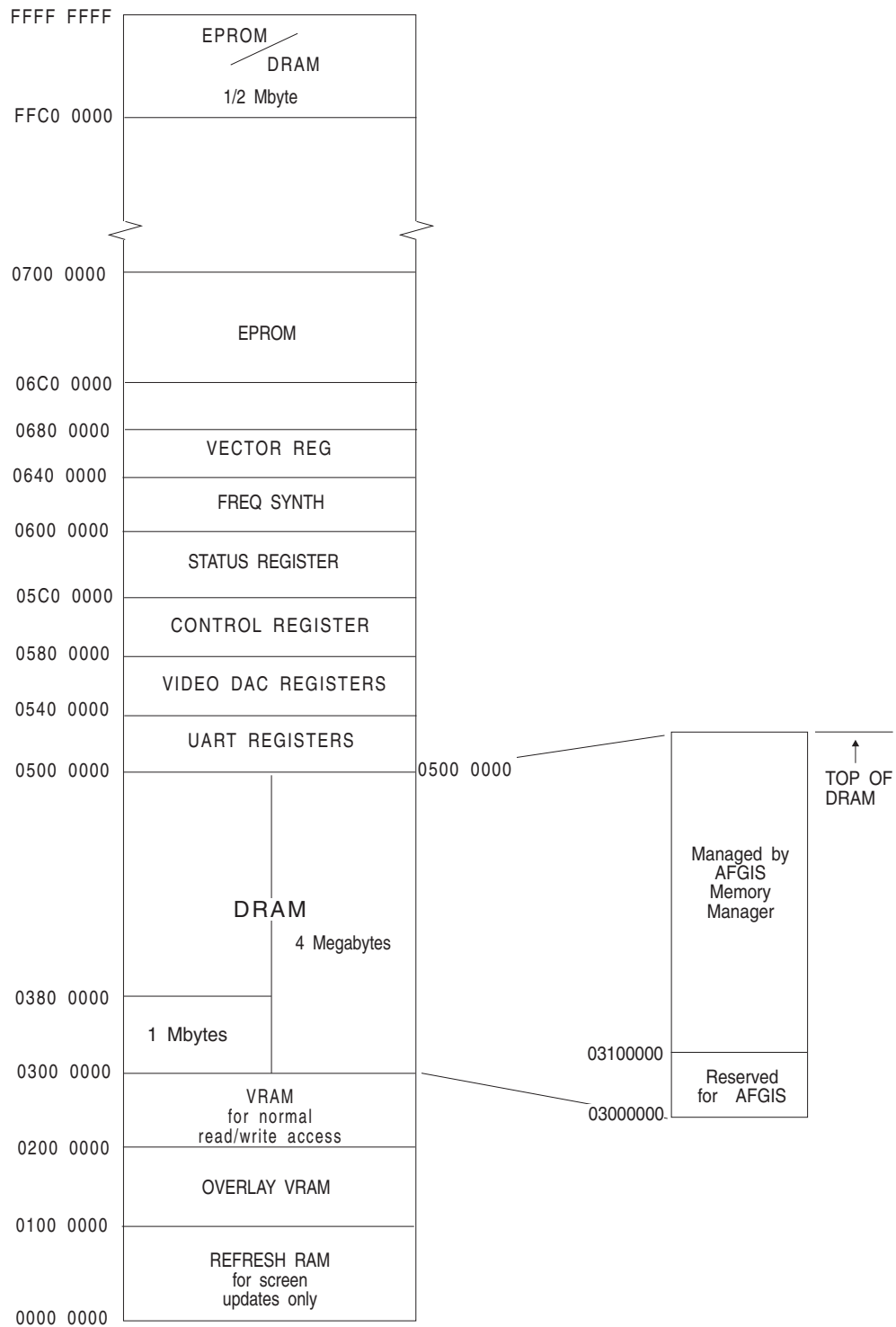
#### HSTCTL

BIT	NAME	DESCRIPTION
15	HLT	Halts TMS34010 processing
14	CF	Flushes the cache
13	LBL	Lower byte last
12	INCR	Increments address after each read
11	INCW	Increments address after each write
10		reserved
9	NMIM	Selects the mode for the nonmaskable interrupt
8	NMI	Enables the nonmaskable interrupt
7	INTOUT	Sends output interrupt from TMS34010 to host
4-6	MSGOUT	Buffers an output message code
3	INTIN	Sets input interrupt from host to TMS34010
0-2	MSGIN	Buffers an input message code

Figure 3.2 Host Interface Registers Bit Assignments

**3.3 RG-751 Memory**

Memory on the RG-751 board includes EPROM, DRAM, video RAM, and memory-mapped registers, as shown in Figure 3.3.



**Figure 3.3 RG-751 Memory Map**

### 3.3 RG-751 Memory (continued)

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#### 3.3.2 EPROM

AFGIS firmware resides in two 27010/27020 EPROMs on the RG-751 graphics boards. U65 is the msb EPROM, which contains data bits D8 through D15. U66 is the lsb EPROM, which contains data bits D0 through D7.

#### 3.3.3 DRAM

The RG-751 can be configured with 1 or 4 Mbytes of DRAM. DRAM is used by AFGIS firmware for instruction storage, for temporary storage of screen data, and for downloaded code. The first 64k words of DRAM are reserved for use by AFGIS firmware. The rest of DRAM, starting at 03100000h, is available for user code, and is managed by the AFGIS memory manager.

The AFGIS memory manager returns an address to the start of a block of DRAM requested by the user with the R\_ALLOC opcode. Memory is allocated starting at the beginning of available DRAM (03100000h).

The default location for downloading and executing AFGIS opcodes is also 03100000h. DRAM at this address and above (AFGIS heap) is controlled by the AFGIS memory manager and will be allocated to the first request for memory with the R\_ALLOC opcode. To avoid memory usage conflict, a block of memory should be requested from the AFGIS memory manager for AFGIS opcode processing (If the R\_ALLOC opcode is never used to allocate memory for any other purpose, AFGIS opcodes can be safely run at 03100000h without allocating memory for opcode processing).

#### 3.3.4 Fixed DRAM Interface

DRAM, starting at 03000000h is designated as Fixed RAM and contains flags, addresses, and parameters for access by the VMEbus host. Fixed RAM values are either 16 or 32 bits long, and may have restricted access. R means the location may be read by the host, but it may not be modified. R/W means that the location may be read from or written to by the host. Fixed RAM is organized as shown on the next page. See the AFGIS programming Manual for additional information.

### 3.3 RG-751 Memory (continued)

ADDRESS	NAME	SIZE	ACCESS	DESCRIPTION
03000000h	EODLFLAG	16	R/W	= 0 when the RG-751 is busy. = 1 when the RG-751 is not busy.
03000010h	KBDFLAG	16	R/W	= 0 when there is no keyboard data. = 1 when keyboard data is in available
03000020h	MSEFLAG	16	R/W	= 0 when there is no mouse/serial data. = 1 when mouse/serial data is in available
03000030h	ERRFLAG	16	R/W	= 0 when no errors have been detected = 1 when an error has been detected
03000040h	IDLEFLAG	16	R/W	Set to 1 on each pass of the idle loop, approximately every 10 usecs. Not cleared by AFGIS firmware.
03000050h	DI_COUNT	16	R	60hz continuous counter, updated by AFGIS.
03000060h	INTOUTMASK	16	R/W	RG-751 to host interrupt enable mask.
03000070h	HOST_FIELD0	16	R/W	Reserved for host use.
03000080h	HOST_FIELD1	32	R/W	Reserved for host use.
030000A0h	ENV_PTR	32	R/W	Address of current graphics environment.
030000C0h	HINT0_AFG_ENTRY	32	R/W	AFGIS display list address. Used by HINT0
030000E0h	HINT1_TMS_ENTRY	32	R/W	TMS assembly code address. Used by HINT1
03000100h	GPTABLE_PTR	32	R	Address of global pointer table
03000120h	DEFAULT_ENV_PTR	32	R	Address of default environment
03000140h	DPAGEADDR	32	R	Current display page address
03000160h	DPAGE	16	R	Current display page number (0,1...)
03000170h	ZOOM	16	R	Underlay plane zoom factor
03000180h	PAN	32	R	Underlay plane starting address

**Figure 3.4 Fixed RAM Parameters**

### 3.3.5 VRAM - Overlay and Underlay Planes

Video RAM, VRAM, holds the image displayed on the video screen. VRAM is normally written to by the TMS34010 graphics processor on the RG-751 as a consequence of AFGIS opcode processing. However, image data can also be downloaded directly into VRAM by the VMEbus host.

VRAM is organized into two planes, an overlay plane and an underlay plane. The overlay plane provides 15 colors. (Color 0 is “transparent” and allows information in the underlay plane to “show through”). The underlay plane provides 16 or 256 colors, and includes hardware pan and zoom. The underlay may be zoomed 1x, 2x, or 4x and may be panned in x or y by pixels. The overlay plane does not support pan or zoom. Information written to the overlay plane obscures data written to the underlay plane (as opposed to mixing with it). The overlay and underlay planes can be independently erased.

### 3.3 RG-751 Memory (continued)

#### 3.3.5 VRAM - Overlay and Underlay Planes (continued)

The underlay plane is organized as a 1K x 1K buffer for 8 bits/pixel configurations, and a 2K x 1K buffer for 4 bits/pixel configurations. The beginning of the underlay plane in VRAM, 0200 0000h, corresponds to the top left corner of the video screen.

The overlay plane is organized as a 1K x 1K buffer for 4 bits/pixel configuration. The beginning of the overlay plane is 0100 0000h, and corresponds to the upper left corner of the video screen.

The overlay and underlay planes are distinguished by a channel ID parameter as follows:

Channel I D	Description
0 100h	underlay channel overlay channel

The INITGCC opcode may be used to initialize a graphics context to generate graphics in either the underlay or overlay plane (default is the underlay plane). The SETPALETTE opcode may be used to re-program either the underlay or overlay palettes, and the MSCSRPAGE opcode may be used to place the mouse cursor in either the underlay or overlay (default is underlay). See the AFGIS programming manual for more information.

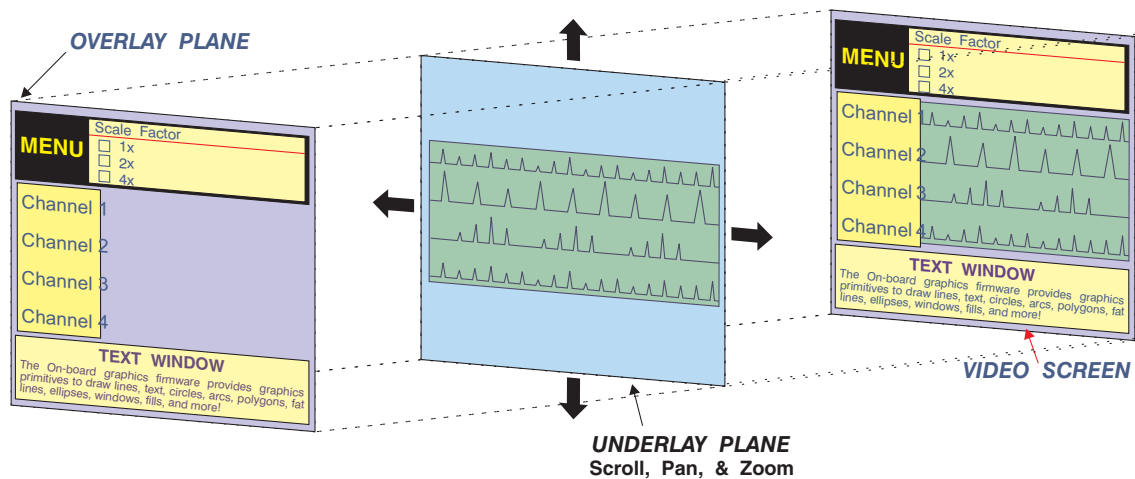


Figure 3.5 Overlay Architecture

### 3.3 RG-751 Memory (continued)

#### 3.3.6 Remapping DRAM with ROMDIS (D13)

The ROMDIS bit, D13, in the Control Register remaps DRAM to the top portion of the address space (see Figure 3.6). This feature allows code to be downloaded into DRAM for execution independent of AFGIS firmware. If 1 Mbyte of DRAM is installed, DRAM is mapped to the top of the address space, starting at FFC00000h. If 4 Mbytes of DRAM are installed, DRAM starts at FF000000h.

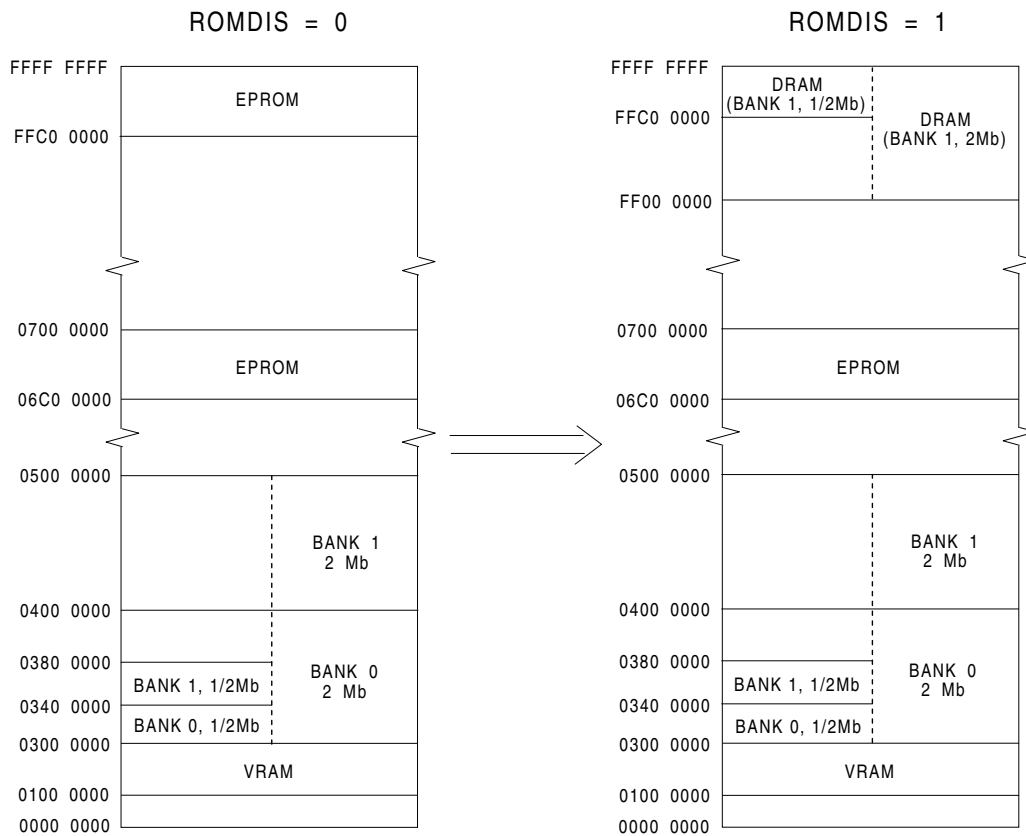


Figure 3.6 EPROM/DRAM Swap

#### 3.3.7 RS-232 Serial Interface

The RS-232 Serial Interface can be used for a serial mouse (with Microsoft format) or it can be used to connect a serial device to the RG-751. The handshake lines (RTS, DTR, etc.) can be reversed at J8 and J9 to allow use of a flat cable connected to a DB9 connector. The serial interface uses the Signetics 2691 UART, which is a programmable device with many options. The bit assignments for the 2691 registers are shown below.

### 3.3 RG-751 Memory (continued)

#### 3.3.8 Programing the 2691 UART

The 2691 Universal Asynchronous Receiver/Transmitter (UART) has quadruple buffered receiver data registers and a fully programmable data format. The baud rate for the receiver and transmitter can be selected from 9 fixed rates. The UART contains eight registers that determine its mode of operation (see Figure 3.7 and Figure 3.8). Refer to the Signetics 2691 UART data sheet for additional information.

ADDRESS	DESCRIPTION	DEFAULT CONTENTS
05000000h	MR1 - Mode Register 1	13h
05000000h	MR2 - Mode Register 2	17h
05000010h	CSR - Channel Status Register	0BBh
05000020h	CR - Command Register	0A5h
05000040h	ACR - Auxillary Control Register	68h
05000050h	ISR - Interrupt Status Register	04h
05000060h	CTUR - Counter Register High	00h
05000070h	CTLR - Counter Register Low	FFh

**Figure 3.7 2691 UART Power Up Register Values**

The 2691 UART is configured by the AFGIS firmware at power up as follows:

- 9600 baud
- 8bits/character
- 1stopbit
- no parity
- Transmit Data line controlled by CTS handshake
- RTS asserted. RTS is deasserted when the receive buffer becomes full.
- DTR always asserted
- DSR always asserted

Use the SERUART opcode to reprogram the 2691.

### 3.3 RG-751 Memory (continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
<b>MR1</b>	RxRTS CONTROL	RxINT SELECT	ERROR MODE	PARITY MODE		PARITY TYPE	BITS PER CHAR	
	0 = no 1 = yes	0=RXRDY 1 = FULL	0 = char 1 = block	00 = with parity 01 = force parity 10 = no parity 11 = special mode		0 = even 1 = odd	00 = 5 01 = 6 10 = 7 11 = 8	
<b>MR2</b>	CHANNEL MODE		Tx RTS CONTROL	Tx CTS ENABLE	STOP BIT LENGTH			
	00 = normal 01 = auto echo 10 = local loop 11 = remote loop		0 = no 1 = yes	0 = no 1 = yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.751	4 = 0.183 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.751	C = 1.813 D = 1.875 E = 1.938 F = 2.000
<b>CSR</b>	RECEIVER CLOCK SELECT				TRANSMITTER CLOCK SELECT			
	ACR (7) = 0: 50 - 38.4k baud ACR(7) = 1: 75 - 19.2k baud				ACR (7) = 0: 50 - 38.4k baud ACR (7) = 0: 50 - 38.4k baud			
<b>CR</b>	MISCELLANEOUS COMMANDS				DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
	see UART data sheet				0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes
<b>ACR</b>	BRG SET SELECT	COUNTER MODE & SOURCE			POWER DOWN MODE	MPO FUNCTION SELECT		
	0 = set1 1 = set2	see UART data sheet			0 = on 1 = off	see UART data sheet		
<b>ISR</b>	MPI PIN CHANGE	MPI PIN STATE		COUNTER READY	DELTA BREAK	RxRDY/FULL	TxEML	TxRDY
	0 = no 1 = yes	0 = low 1 = high	not used	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes
<b>CTUR</b>	8 MSBs OF COUNTER/TIMER VALUE							
<b>CTLR</b>	8 LSBs OF COUNTER/TIMER VALUE							

Figure 3.8: 2691 UART Register Contents

#### 3.3.9 Keyboard Interface

An AT style keyboard can be connected to the RG-751 at J14. An adapter cable is required to connect from the DB9 on the RG-751 to the keyboard 5 pin DIN connector. AFGIS firmware decodes the keyboard scan codes, stores the ASCII codes in RAM, and informs the VMEbus host of available keyboard data via an interrupt or a polling register in fixed RAM.

### 3.3 RG-751 Memory (continued)

#### 3.3.10 Video DAC (Bt478)

RS-343 video is generated by the RG-751 with a Bt478 type Video DAC. The Video DAC has a 256 x 24 color look up table (used by the underlay plane), allowing a user to select 256 colors from a palette of 16 million. The overlay plane connects to the overlay interface on the BT478 and provides 15 colors (color 0 is “transparent”). The Video DAC registers are located as shown below:

UNDERLAY PLANE		OVERLAY PLANE	
ADDRESS	DESCRIPTION	ADDRESS	DESCRIPTION
05400000h	Write Address Register	05440000h	Overlay Write Address Register
05410000h	Data Register	05450000h	Overlay Data Register
05420000h	Pixel Read Mask Register	05460000h	(reserved)
05430000h	Read Address Register	05470000h	Overlay Read Address Register
02000000h	Underlay Plane	01000000h	Overlay Plane

**Figure 3.9 Video DAC Registers**

#### 3.3.11 Control Register

The RG-751 has a Control Register to control on-board hardware functions. The Control Register is located at 05800000h and has the following bit assignments. Use the CONTREGX opcode to modify the contents of the Control Register.

D15	Red Led	0 = off, 1= on
D14	Debug Enable	0 = off, 1= on
D13	* ROMDIS	0 = EPROM 1= RAM
D12	* Vsync Polarity	0 = active low 1 = active high
D11	* Hsync Polarity	0 = active low 1 = active high
D10	LNINT	
D9	FCLREN	
D8	Green Led	0 = off, 1= on
D7	* Sync on Green	0 = sync on green 1 = no sync on green
D6	Keyboard Serial Data	
D5	Keyboard clock	
D4	Memory Devices Installed	0 = 1 Mbyte 1 = 4 Mbyte
D3	8 bit video.	0 = 4 bit video 1 = 8 bit video
D2	Not used	
D1	Not used	
D0	Not used	

*\*These bits are user configurable with the CONTREGX opcode.*

**Figure 3.10 Control Register Bit Assignments**

### 3.3.12 Status Register

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The Status Register, located at memory address 05C00000h, provides information on the current state of RG-751 operations (see Figure 3.11).

<b>BIT</b>	<b>DESCRIPTION</b>
D0	configuration jumper
D1	configuration jumper
D2	configuration jumper
D3	configuration jumper
D4	sync on green jumper
D5	keyboard clock
D6	keyboard data
D7	hsync polarity jumper
D8	vsync polarity jumper
D9	debug enable jumper

**Figure 3.11 Status Register**

## 3.4 Interrupts

---

Interrupts are sent to the RG-751 from the VMEbus host to initiate display list processing, to run TMS34010 code, and to reset the RG-751.

Interrupts can also be sent from the RG-751 to the VMEbus host to indicate the completion of display list processing, to indicate that RS-232, mouse, or keyboard data is ready, to indicate a 60Hz interrupt, or to indicate an error condition.

### 3.5 Interrupts to the RG-751 from the VMEbus

Interrupts are sent to the RG-751 by setting the appropriate bits in the HSTCTL register, located at TMS34010 address C0000100h or at VMEbus Host Interface Register address xxxx06h. Two types of interrupts can be sent to the RG-751 from the host CPU via the HSTCTL register: host interrupts and non-maskable interrupts.

BIT	NAME	DESCRIPTION
15	HLT	Halts TMS34010 processing
14	CF	Flushes the cache
13	LBL	Lower byte last
12	INCR	Increments address after each read
11	INCW	Increments address after each write
10		(reserved)
9	NMIM	Selects the mode for the nonmaskable interrupt
8	NMI	Enables the nonmaskable interrupt
7	INTOUT	Sends output interrupt from TMS34010 to host
4-6	MSGOUT	Buffers an output message code
3	INTIN	Sets input interrupt from host to TMS34010
0-2	MSGIN	Buffers an input message code

**Figure 3.12 HSTCTL Bit Assignments**

### 3.5 Interrupts to the RG-751 from the VMEbus (continued)

#### 3.5.1 Host Interrupts to the RG-751

Host interrupts are sent to the RG-751 via the VMEbus, and are used to initiate display list processing and execute TMS34010 code. A host interrupt is asserted by setting bit D3 (INTIN)=1 in the TMS34010 HSTCTL register. A host interrupt is identified by bits D(0-2) (MSGIN) in the HSTCTL register. Use HINT0 to execute a display list starting at the address contained in HINT0\_AFG\_ENTRY located at address 030000C0h (its default value is 03100000h). HINT0 is asserted by writing 0008h to the HSTCTL register, at the default address, E00006h. HINT1 is asserted by writing 0009h to HSTCTL. Use HINT1 to execute TMS34010 assembly code at the address contained in HINT1\_TMS\_ENTRY located at address 030000E0h (its default value is also 03100000h).

MSGIN NUMBER	MSGIN NAME	HSTCTL			DESCRIPTION
		D2	D1	D0	
0	HINT0	0	0	0	Process AFGIS opcodes beginning at the address specified in HINT0_AFG_ENTRY (at RAM location 0300 00C0h). The default address in HINT0_AFG_ENTRY is 03100000h.
1	HINT1	0	0	1	Process TMS34010 opcodes at address specified in HINT1_TMS_ENTRY (at RAM location 0300 00E0h). The default address is HINT1_TMS_ENTRY is 03100000h.
2	HINT2	0	1	0	reserved
3	HINT3	0	1	1	reserved
4	HINT4	1	0	0	reserved
5	HINT5	1	0	1	reserved
6	HINT6	1	1	0	reserved
7	HINT7	1	1	1	reserved

Figure 3.13 Host Interrupts to RG-750

#### 3.5.2 Resetting The RG-751 With The NMI Interrupt

An NMI interrupt with message value 1 may be used to abort display list processing, and cause the RG-751 to enter the idle loop. NMI 1 does not affect DRAM parameters

An NMI interrupt with a message value of 0 totally resets the RG-751, putting it into a power up condition.

An NMI interrupt is issued by setting the NMI bit, D8, in the HSTCTL register and by setting the appropriate message bits in D0-D2.

### 3.6 Interrupts to the VMEbus from the RG-751

The RG-751 can send an interrupt to the VMEbus host by setting D7=1 in HSTCTL along with a 3 bit code (D4 - D6) identifying the different interrupt (see Figure 3.14). The interrupts are individually enabled or disabled by setting the corresponding bits in the INTOUTMASK RAM location (03000060h). The code (or message number) for the interrupt is determined by bits D4-D6 in the HSTCTL register and identifies 1 of 8 interrupts. The VMEbus interrupt service routine would normally read the HSTCTL register to determine which of the eight interrupts occurred. *On exit, the interrupt service routine **must** clear HSTCTL bit D7 (set D7=0), as the RG-751 will not issue another interrupt until bit D7 in HSTCTL has been **cleared**.*

MSGOUT NUMBER	MSGOUT NAME	INTOUTMASK BIT	HSTCTL			DESCRIPTION
			D6	D5	D4	
0	RGIOUT0	D0	0	0	0	An AFGIS EODL instruction has been executed
1	RGIOUT1	D1	0	0	1	A character is ready from the keyboard port.
2	RGIOUT2	D2	0	1	0	Data is ready from the serial/mouse port.
3	RGIOUT3	D3	0	1	1	An error has occurred and is recorded in DRAM.
4	RGIOUT4	D4	1	0	0	An interrupt is generated at approximately 60 Hz.
5	RGIOUT5	D5	1	0	1	Reserved
6	RGIOUT6	D6	1	1	0	Reserved.
7	RGIOUT7	D7	1	1	1	Reserved.

**Figure 3.14** Interrupt Output Messages to VMEbus

**Note:** *HSTCTL is a 16 bit register located at the -PS25 default address E00006h, and has the bit assignments shown in Figure 3.12. When viewed from the TMS34010 side, HSTCTL appears as two 16 bit registers, HSTCTLH and HSTCTLH, with each register containing half the data bits (in the same bit positions as shown for HSTCTL) that are in HSTCTL. HSTCTLH is located at C0000F0h, and HSTCTLH is located at C000100h.*

BIT	NAME	DESCRIPTION
8-15	Reserved	Not Used
7	INTOUT	Sends output interrupt from TMS34010 to host
4-6	MSGOUT	Buffers an output message code
3	INTIN	Sets input interrupt from host to TMS34010
0-2	MSGIN	Buffers an input message code

**Figure 3.15**  
HSTCTLH located at C0000F0h

BIT	NAME	DESCRIPTION
15	HLT	Halts TMS34010 processing
14	CF	Flushes the cache
13	LBL	Lower byte last
12	INCR	Increments address after each read
11	INCW	Increments address after each write
10		(reserved)
9	NMIM	Selects the mode for the nonmaskable interrupt
8	NMI	Enables the nonmaskable interrupt
0-7	Reserved	Not Used

**Figure 3.16**  
HSTCTLH located at C000100h

### 3.6 Interrupts to the VMEbus from the RG-751 (continued)

The RG-751 generates an interrupt to the VMEbus when HSTCTL bit D7 is set to 1 and if the corresponding message value is enabled by INTOUTMASK. When D7=1 in HSTCTL, the HINT line, which is connected to the VMEbus interrupt line via a PAL, is enabled active low, initiating the interrupt. The VMEbus interrupt line used by the PAL (IRQ 1-7) is selected using jumper J1. An 8-bit interrupt vector register, located at TMS34010 address 06400000h, is programmed by the VMEbus host with its appropriate vector, and the vector is placed on the data bus in response to an interrupt acknowledge signal.

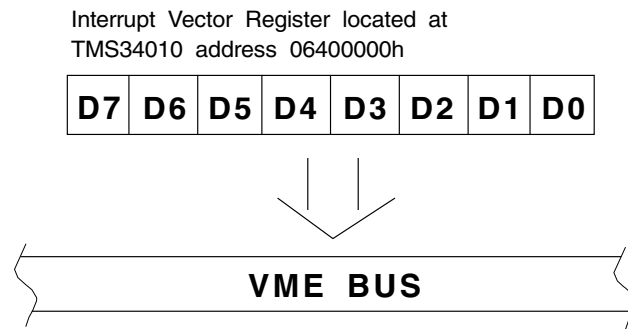


Figure 3.17 Interrupt Vector Register

### 3.7 Coordinate System

The screen coordinates are shown in Figure 3.18. 0,0 is in the upper left, x increases to the right, and y increases downward.

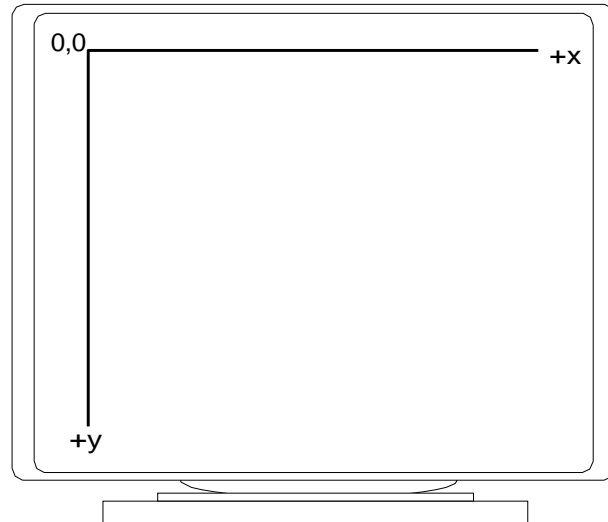


Figure 3.18 Display Coordinate System

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## 4.0 SPECIFICATIONS

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### Chapter Contents:

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- 4.1 Operating Environment
- 4.2 DC Power Requirements
- 4.3 Video Output
- 4.4 Video Timing

## 4.1 Operating Environment

---

Operating Temperature: 0°C to 55°C

Storage Temperature: -40°C to 65°C

Relative Humidity: 0% to 95% (non-condensing)

Altitude: 7500 ft.

## 4.2 DC Power Requirements

---

+ 5V at 3.8 Amps

+12V at 0.2 Amps

- 12V at 0.2 Amps

When the Planar E17768MS electroluminescent flat panel is connected to the RG-751, the following additional DC power is required:

+ 5V at .2 Amps

+12V at 2.0 Amps

## 4.3 Video Output

---

Analog 1.0V, RS-343 video, with sync on green and sync polarity (options) is output at DB15, J13 and at optional BNC connectors J10, J11, & J12.

## 4.4 Video Timing

---

The RG-751 video timing is resolution dependent, as shown in Figures 4.1 through 4.3

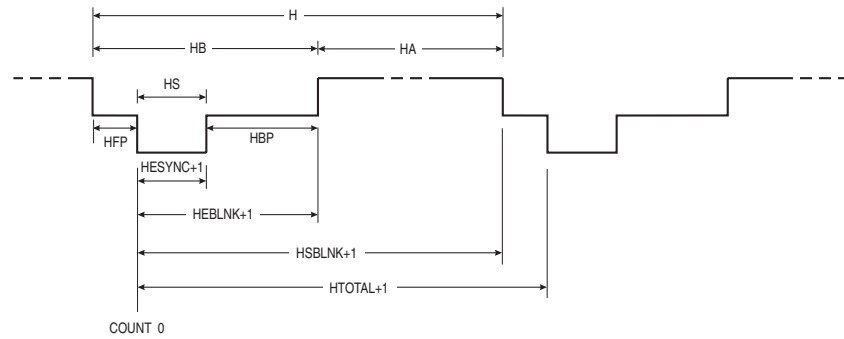


Figure 4.1 Horizontal Video Timing

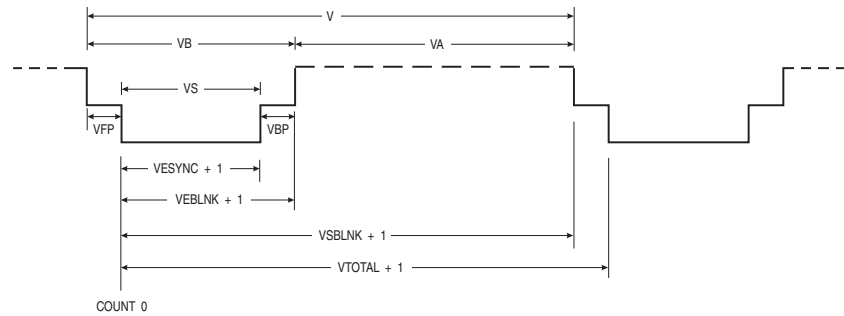


Figure 4.2 Vertical Video Timing

	640h x 480v	640h x 480v EL7768MS	800h x 600v	1024h x 768v
<b>PCLOCK</b>	25.175MHz	25.175 MHz	36.000MHz	63.960MHz
<b>HFREQ</b>	31.468KHz	31.468KHz	35.156KHz	48.454KHz
<b>H</b>	31.777µs	31.777µs	28.444µs	20.638µs
<b>HS</b>	3.4957µs	3.813µs	2.000µs	1.001µs
<b>HBP</b>	1.90µs	1.588µs	3.555µs	2.877µs
<b>HA</b>	25.422µs	25.422µs	22.222µs	16.010µs
<b>HFP</b>	0.953µs	0.953µs	0.666µs	0.758µs
<b>HB</b>	6.333µs	6.333µs	6.222µs	4.628µs
<b>VFREQ</b>	59.940Hz	59.940Hz	56.250Hz	59.968Hz
<b>V</b>	16,683µs	16,683µs	17,777µs	16,675µs
<b>VS</b>	63µs	63µs	56µs	82µs
<b>VBP</b>	1,016µs	762µs	625µs	661µs
<b>VA</b>	15,253µs	15,761µs	17,060µs	15,850µs
<b>VFP</b>	349µs	95µs	28µs	82µs
<b>VB</b>	1,430µs	922µs	717µs	825µs
<b>HESYNC</b>	10 (000A)	11 (000B)	8 (0008)	7 (0007)
<b>HEBLNK</b>	16 (10010)	16 (10010)	24 (0018)	30 (001E)
<b>HSBLNK</b>	96 (0060)	96 (0060)	124 (007C)	158 (009E)
<b>HTOTAL</b>	99 (0063)	99 (0063)	127 (007F)	164 (00A4)
<b>VESYNC</b>	1 (0001)	1 (0001)	1 (0001)	3 (0003)
<b>VEBLNK</b>	33 (0021)	25 (0019)	23 (0019)	35 (0023)
<b>VSBLNK</b>	513 (0201)	521 (0209)	623 (026F)	803 (0323)
<b>VTOTAL</b>	524 (020C)	524 (020C)	624 (0270)	807 (0327)

Figure 4.3 Video Timing

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# APPENDIX A

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## Chapter Contents:

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**RG-751 Interface Pal Equations**

**Interface PAL Set, U15 and U14**

**High Address PAL  
Low Address PAL**

**RG-751 Interface PAL Set, U14 and U15.**

This appendix contains the PAL equations, written in PALASM format, for the -PS25 PAL set. The PALs U14 and U15 may be reprogrammed by the user to locate the RG-751 at a different location in VMEbus address space.

The RG-751 is located in VMEbus address space with the interface PALs U14 and U15. The U14 and U15 decode a 256 byte page in VMEbus address space. The RG-751 Host Interface Registers are located in this 256 byte page.

The default PAL set, U14 and U15 (-PS25) locates the RG-751 at E00000h or at E0000000h, depending on the jumper configuration of J3.

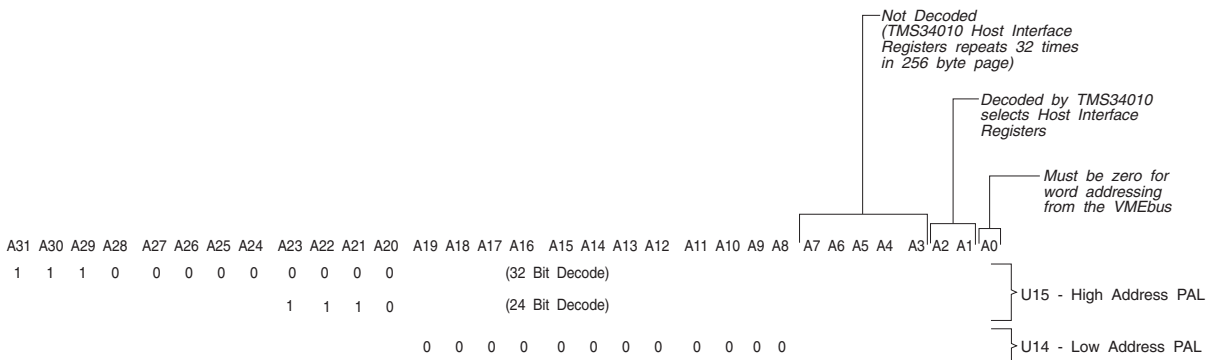
U15 decodes the AM lines and the upper 12 address lines, A20-A31. The AM decode determines the data transfer modes that the RG-751 will respond to. The -PS25 PAL U15 decodes the following AM codes:

32-BIT ADDRESS	24-BIT ADDRESS	
0E	3E	Standard Supervisory Program Access
0D	3D	Standard Supervisory Data Access
0A	3A	Standard Non-privileged Program Access
09	39	Standard Non-privileged Data Access

The address line A20-A31 decode a 1M block of memory. In the case of the -PS25 PAL, U15 decodes a 1M block of memory starting at E00000h or E0000000h, depending on the jumper configuration of J3.

U14 decodes address lines A8-A19, which selects a 256 byte page within the 1M block decoded by U15. In the case of the -PS25 PAL, U14 decodes the first page (0) of 256 bytes in the 1M block. Thus, the RG-751 is located at E00000h or at E0000000h.

Both PALs are required to decode the complete 24 bit or 32 bit addresses. The address decoding is split between the PALs. The decoding for the -PS25 PAL set is shown below.



Title RG-751 High Address Decode PAL  
 Pattern hiaddr.pds  
 Revision 1.0  
 Author G. H.  
 Company Rastergraf, Inc.  
 Date 13 October 1993

```
; PAL Type:          20L8B (15 nsec)
; Board Location:    U22
; Schematic Page:   1
```

```
Chip          HIADDR          PAL20L8

;   1[I]      2[I]      3[I]      4[I]      5[I]      6[I]
   AM5        AM4        AM3        AM2        AM1        AM0

;   7[I]      8[I]      9[I]     10[I]     11[I]     12[GND]
   VA31      VA30      VA29      VA28      VA27      GND

;   13[I]     14[I]     15[O]     16[I/O]   17[I/O]   18[I/O]
   VA26      VA25      /HIDEC    VA24      VA23      VA22

;  19[I/O]   20[I/O]   21[I/O]   22[O]     23[I]     24[VCC]
   VA21      VA20      /SEL      /AMDEC    /IACK     VCC
```

Equations

```
; 24 BIT ADDR:
;   3E -STANDARD SUPERVISORY PROGRAM ACCESS
;   3D -STANDARD SUPERVISORY DATA ACCESS
;   3A -STANDARD NONPRIVILEGED PROGRAM ACCESS
;   39 -STANDARD NONPRIVILEGED DATA ACCESS
; 32 BIT ADDR:
;   0E -STANDARD SUPERVISORY PROGRAM ACCESS
;   0D -STANDARD SUPERVISORY DATA ACCESS
;   0A -STANDARD NONPRIVILEGED PROGRAM ACCESS
;   09 -STANDARD NONPRIVILEGED DATA ACCESS

AMDEC = /SEL * AM5 * AM4 * AM3 * AM2 * AM1 * /AM0 ;3E
+ /SEL * AM5 * AM4 * AM3 * AM2 * /AM1 * AM0 ;3D
+ /SEL * AM5 * AM4 * AM3 * /AM2 * AM1 * /AM0 ;3A
+ /SEL * AM5 * AM4 * AM3 * /AM2 * /AM1 * AM0 ;39
+ SEL * /AM5 * /AM4 * AM3 * AM2 * AM1 * /AM0 ;0E
+ SEL * /AM5 * /AM4 * AM3 * AM2 * /AM1 * AM0 ;0D
+ SEL * /AM5 * /AM4 * AM3 * /AM2 * AM1 * /AM0 ;0A
+ SEL * /AM5 * /AM4 * AM3 * /AM2 * /AM1 * AM0 ;09

HIDEC = /SEL * /IACK * VA23 * VA22 * VA21 * /VA20 ;
+ SEL * /IACK * VA31 * VA30 * VA29 * /VA28 * ;
   /VA27 * /VA26 * /VA25 * /VA24 *
   /VA23 * /VA22 * /VA21 * /VA20
```

```
Title           RG-751 Low Address Decode
PAL Pattern     loadr.pds
Revision        1.0
Author          G.D.H.
Company         Rastergraf, Inc.
Date            13 October 1993
```

```
; PAL Type:           20L8B (15 nsec)
; Board Location:     U11
; Schematic Page:    1
```

```
Chip           LOADDR                               PAL20L8

;   1[I]       2[I]       3[I]       4[I]       5[I]       6[I]
;   /HIDEC     /AMDEC     VA19        VA18        VA17        VA16

;   7[I]       8[I]       9[I]       10[I]      11[I]      12[GND]
;   VA15       VA14       VA13       VA12       VA11       GND

;   13[I]      14[I]      15[O]      16[I/O]    17[I/O]    18[I/O]
;   VA10       VA9        /ADEC      /HCS       nc         /AS

;   19[I/O]    20[I/O]    21[I/O]    22[O]      23[I]      24[VCC]
;   /RESET     /HALT     /SEL      SRESET    VA8        VCC
```

## Equations

```
SRESET = RESET
```

```
; *****
; *** NOTE: The address decodes in ADEC and HCS MUST be identical ***
; *****
```

```
; HCS is a complete decode of AM[5..0] and VA[31..8] and AS qualified by
; RESET. HCS is also asserted during RESET if the HALT jumper is not IN.
```

```
HCS = /SEL * /RESET * HIDEC * AMDEC * AS * ;Address Select Jumper OUT
      /VA19 * /VA18 * /VA17 * /VA16 * ;Address Select 0
      /VA15 * /VA14 * /VA13 * /VA12 * ;
      /VA11 * /VA10 * /VA9 * /VA8 ;
+ SEL * /RESET * HIDEC * AMDEC * AS * ;Address Select Jumper IN
      /VA19 * /VA18 * /VA17 * /VA16 * ;Address Select 1
      /VA15 * /VA14 * /VA13 * /VA12 * ;
      /VA11 * /VA10 * /VA9 * /VA8 ;
+ RESET * /HALT ; Halt Jumper OUT
```

```
; ADEC is identical to HCS except that it is not asserted during RESET
```

```
ADEC = /SEL * /RESET * HIDEC * AMDEC * AS * ;Address Select Jumper OUT
        /VA19 * /VA18 * /VA17 * /VA16 * ;Address Select 0
        /VA15 * /VA14 * /VA13 * /VA12 * ;
        /VA11 * /VA10 * /VA9 * /VA8 ;
+ SEL * /RESET * HIDEC * AMDEC * AS * ;Address Select Jumper IN
      /VA19 * /VA18 * /VA17 * /VA16 * ;Address Select 1
      /VA15 * /VA14 * /VA13 * /VA12 * ;
      /VA11 * /VA10 * /VA9 * /VA8 ;
```

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## APPENDIX B

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### Chapter Contents:

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**Transferring Data from 680x0 Memory to  
TMS34010 Memory  
Data in 680x0 Memory  
Transferring Bytes  
Transferring Words  
Transferring Longs**

**Transferring Data from 680x0 memory to TMS34010 memory**

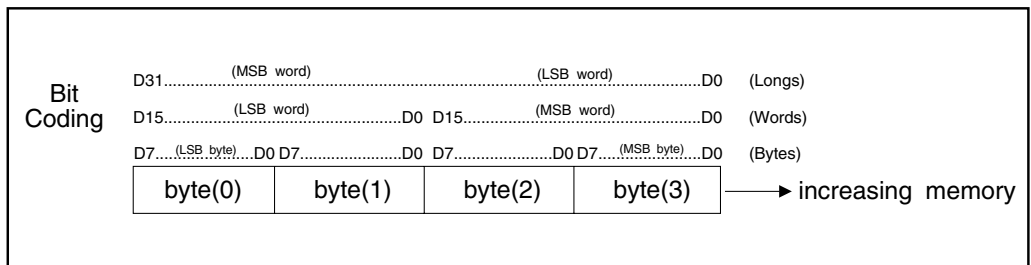
The following discussion describes how data should be transferred from 680x0 memory via the VMEbus to TMS34010 memory on Rastergraf, Inc. graphics boards.

This discussion is primarily intended for users who want to develop their own interface to the graphics board.

Rastergraf, Inc. software products such as the AFGIS C Graphics Library and AFGIS Assembler perform the necessary data manipulations to make the interface transparent to the user.

**Data in 680x0 Memory**

Data in 680x0 memory is typically described as shown in Figure B.1, and can be bytes, words, or longs. Bytes are numbered left to right (in the direction of increasing memory) and are identified as byte(0), byte(1), byte(2), and byte(3) and have the corresponding 680x0 hex addresses xxxxx0, xxxxx1, xxxxx2, and xxxxx3 (or xxxxxxx0, etc. for 32 bit addressing mode).



**Figure B.1 680x0 Bit and Byte Numbering Conventions**

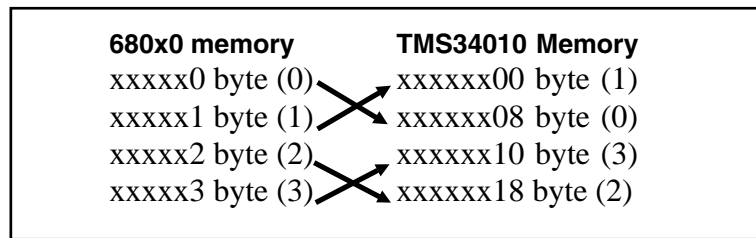
Sixteen bit data (two bytes) are transferred across the VMEbus as shown in Figure B.2.

680x0	VMEbus Data Lines	
Byte Locations	D15-D8	D7-D0
byte(0-1)	byte (0)	byte (1)
byte(2-3)	byte (2)	byte (3)

**Figure B.2 16-Bit Data Transfers Across the VMEbus**

**Data in 680x0 Memory (continued)**

Data may only be transferred to or from Rastergraf, Inc. TMS34010 based graphics boards 16 bits at a time, and only with one of the two byte sets; byte(0), byte(1) or byte(2), byte(3). Figure B.3 shows how a long (32 bits) would be transferred from 680x0 memory to long aligned TMS34010 memory (the start address in TMS34010 memory could be any bit value, but AFGIS firmware requires that the AFGIS opcodes be loaded on word boundaries).



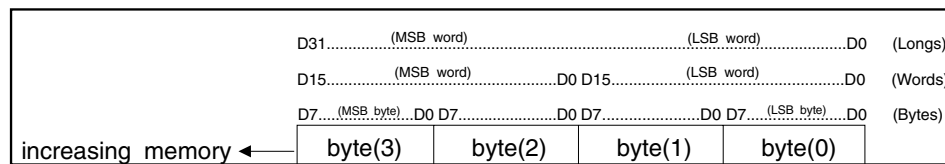
**Figure B.3 32 Bit Data Transfers**

In Figure B.1, byte(0) is the lsb byte in the byte sequence byte(0), byte(1), byte(2), and byte(3). For words, byte (0), byte(1) is the lsb word, and byte(2), byte(3) is the msb word (the next word). For a long, all four bytes are used to represent the long, and the byte pair byte(0), byte(1) is the msb word of the long, and byte pair byte(2), byte(3) is the lsb word of the long.

The two byte pairs byte(0), byte(1) and byte(2), byte(3) that may be transferred across the VMEbus to the graphics board have a different meaning for the data types bytes, words, and longs.

Our objective, for successful data transfer, is to maintain the order of bytes, words, and longs when the data is transferred from 680x0 memory to TMS34010 memory.

Data in TMS34010 memory is typically described as shown in Figure B.4.



**Figure B.4 TMS34010 Bit and Byte Numbering Conventions**

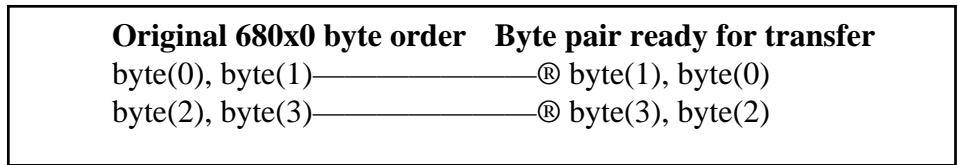
In Figure B.4, byte(0) is the lsb byte in the byte sequence byte(0), byte(1), byte(2), and byte(3). For words, byte(1), byte(0) is the lsb word, and byte(3), byte(2) is the msb word (the next word). For a long, all four bytes are used to represent the long, and byte pair byte(3), byte(2) is the msb word of the long, and byte(1), byte(0) is the lsb word of the long.

**Data in 680x0 Memory (continued)**

As can be seen by examining Figures B.1, B.2, B.3, and B.4, data transferred from 680x0 memory directly to TMS34010 memory without modification only meets our objective if the data being transferred are words.

**Transferring Bytes**

If the data being transferred are bytes, it is evident that the byte pairs byte(0), byte(1) or byte(2), byte(3) end up in the wrong order in TMS34010 memory. The solution is to swap the order of the bytes before the byte pair is transferred across the VMEbus as shown in Figure B5.



**Swapping Byte Order for Transfer of Bytes Across the VMEbus**

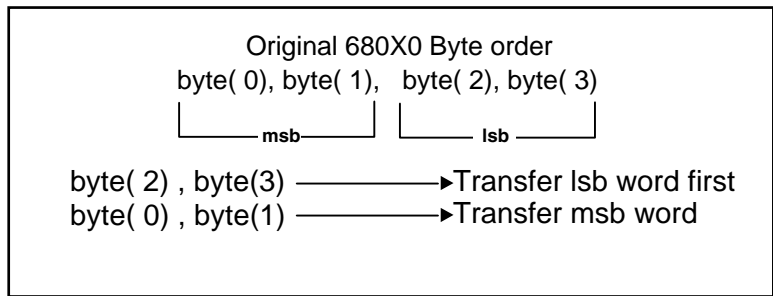
**Figure B.5**

**Transferring Words**

If the data being transferred across the VMEbus are words, the data may be transferred without modification, as can be seen by examining Figures B1, B2, B3, and B4.

**Transferring Longs**

If the data being transferred across the VMEbus are longs, it is evident from Figures B1, B2, B3, and B4 that the msb and lsb words of the long are interchanged if transferred to TMS34010 memory directly from 680x0 memory without additional processing. The solution is to transfer the lsb word first [byte(2), byte(3)], and then transfer the msb word [byte(0), byte(1)] as shown in Figure B6.



**Figure B.6 Transferring a Long Word**