VME64x Live Insertion System Requirements Draft Standard

VITA 1.4-200x

Draft 0.6
March, 17 2000

This draft standard is being prepared by the VITA Standards Organization (VSO) and is unapproved.

Do not specify or claim conformance to this draft standard.

VITA Standards Organization
7825 East Gelding Drive, Suite 104
Scottsdale, AZ 85260
Ph: 480-951-8866 Fx: 480-951-0720
URL:http://www.vita.com

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Abstract

The design requirements in this standard permits Live Insertion compliant VME64x boards to be removed from or inserted into powered and operating subracks. This document contains design requirements for 3U, 6U, and 9U live insertable boards, backplanes, and system that accomplishes that feature. This standard also describes the software and hardware needed to support broad usability and to avoid system stoppages due to transient bus errors. This standard is based upon the VITA 1.1-1998 VME64 Extensions standard.

Foreward

(This foreward is not part of the VITA standard)

The emerging market for open, scaleable, reconfigurable and maintainable system components provides the incentive for developing VME64x-based products designed for high functionality and quality. In addition, there is strong and rising demand for systems that allow adding to, removing from and changing the system configuration while it is functioning. The additional capabilities available via the 160 pin, 5 row, DIN-style connectors as specified in VITA 1.1-1998 VME64 Extensions draft standard make VME live insertion possible. VITA 1.4-200x specifies the application of existing and new hardware and software technologies in order to solve the issues of live insertion of VME64x boards based boards into a VME64x based subrack and backplane. The standard specifies hardware and software elements that are a superset of the VITA 1.1-1998 VME64 Extensions Standard.

The live insertion technologies described herein are based upon pioneering work done by IBM, without whose efforts this standard may not have been possible. Much of the remainder of these requirements were developed by the High Availability task group of the VSO, Wayne Fischer (FORCE Computers), moderator. As philosophical issues delayed the VME High Availability standard, the ability to perform live insertion in a VME based system was deemed too important to delay any further and the H.A. VME standard was excerpted to form the foundation for this document. Further credit for pioneering work in live insertion methods was done by a task group, Moderated by Robert McKee (MITRE Corp.), that resulted in the standard Board Level Live Insertion for VMEbus standard ANSI/VITA 3-1995.

This standard was processed and submitted to the Live Insertion Task Group ("the group") of the VITA Standards Organization (VSO). The VSO is the technical standards development body of the VMEbus International Trade Association (VITA) of Scottsdale, AZ, USA. The group unanimously approved this standard by formal ballot. At the time of the approval of this standard the committee had the following members:

Ray Alderman, Executive Director of the VMEbus International Trade Association (VITA)
John Rynearson, Technical Director of VITA.
Robert W. Downing, VITA Standards Organization (VSO) Chairman
Louis Francz, Moderator, Dialogic Corp., Parsippany, NJ

Organizations Represented:

NAME	COMPANY
Drew Bearding	Arizona Digital
Joe Bedard	Hewlett-Packard Company
James Botte	Nortel Networks
Martin Blake	APW Electronic Solutions
Robert Downing	Fermi National Accelerator Lab
Douglas Endo	Raytheon Systems Company
Lou Francz	Dialogic Corporation
Frank Hom	APW Electronic Solutions
Jonathan Jones	Interactive Circuits & Systems

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Jing Kwok	DY 4 Systems, Inc.
Tony Lavely	Mecury Computer Systems, Inc.
Patrick Mchugh	ARMY Research Laboratory
Jonathan Morris	Tundra Semiconductor Corporation
James Pangburn	Fermi National Accelerator Lab
Jerry Pongstaporn	Ariel Corporation
Dave Robak	Harting, Inc of North America
Dick Somes	Force Computers
Morton Thayer	Cmac
Michael Thompson	Pentair Electronic Packaging
Istvan Vadasz	Force Computers GmbH
David Wright	Transelectric, Ltd.

Comments , Corrections and/or Additions

Anyone wishing to provide comments, corrections and/or additions to this proposed standard, please direct them to the task group chair and draft editor:

Lou Francz, Chair
VME64x Live Insertion System Requirements
Dialogic Corporation
1515 Route 10
Parsippany, NJ 07054
Ph: 201-993-9000 ext. 6125
Fx: 201-993-3093
Em: franczl@dialogic.com

Michael Thompson, Draft Editor
Pentair Electronic Packaging
170 Commerce Drive
Warwick, RI 02818
Ph: 401-732-3770 ext. 397
Fx: 401-739-7599
Em: mthompson@pentair-ep.com

The best way to provide corrections and small additions is via marking up the specific pages and faxing them to the chair and draft editor. For longer additions, the chair prefers to receive just textual information via e-mail.

VSO and Other Standards

Should anyone want information on other standards being developed by VSO, VME Product Directories, VME Handbooks, or general information on the VME market, please contact the VITA office at the address or phone number given on the front cover.

Change Bars

All paragraphs changed in this draft are marked with a change bar on the right side of the Paragraph. Any table entry that was changed will have a bar on the right side of changed entry.

Draft Summary

This is the sixth draft of this standard. Original content of this draft standard was presented and agreed upon at the March 19 & 20, 1997 VSO meeting.
See the draft history for a summary list of the major changes made to each draft.

Draft History

Draft No.	Date	Comments & Major Changes/Updates
D0.1	13 March, 1997	First draft of proposed document
D0.2	7 May, 1997	Format update, correct pinout in table 4-1
D0.3	15 July, 1997	Added LI/I Pin Definition

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D0.4	7 November, 1997	Added Insertion and Removal Process Editorial Changes
D0.5	1 December, 1998	Incorporated changes from Ballot Review Added details to daisy-chain module Removed requirement (3) from Rule 4.1
D06	17 March, 2000	Incorporated changes from Ballot Review

1. Introduction to Live Insertion Concepts

1.1 Definitions

BIST: Built-In Self Test. A set of board resident diagnostic routines that can exercise some or all on-board functional sections.

CSM: Central Services Module. An alternate designation for a slot 1 SysCon module that can also include centralized bus grant and interrupt priority resolution circuits.

DIN-style Connector: In this context, VME board and backplane connectors derived from, and compatible with, the 32 pin by 3 or 5 row, 0.1 inch pitch connectors described in the IEC 60603-2 and IEC 61076-4-113 standards.

Fault Tolerance: The ability of a system to tolerate or recover from the failure of one or more hardware or software elements. A baseline for considering a system fault tolerant is when the failure of a single hardware or software element will not affect the system's ability to perform the designed function.

FRAME Ground: A connection from the chassis to the building's grounding system. This ground is usually isolated from logic ground in the chassis.

High Availability: In this context, systems which are capable of performing their designed functions for a high percentage of the time. This system metric is defined by:

$$\text{Availability} = \frac{\text{Mean Time Before Failure}}{\text{Mean Time Before Failure} + \text{Mean Time To Repair}}$$

The availability number is a probability statistic and is equivalent to a decimal fraction of full time. A common US telephone network availability requirement statistic is 0.99999 or, in other words, available 99.999% of the time. This means that a system that is to be 0.99999 available can have no more than 5 minutes and 15 seconds of system "unavailable" or "down time" per year.

Incident wave switching: A characteristic of a bus driver in a printed wiring backplane environment that exhibits a full amplitude signal edge propagating to all bus boards without waiting for the reflected wave to reinforce the incident wave. Incident waves do not cross the receiver switching threshold because of reflected waves. This condition generally requires controlled slew rate, high current drivers, low stub (board) loading and a low capacitance, higher impedance backplane.

Injector/Extractor: In this context, mechanical levers mounted at the ends of a VME board faceplate that ease both board insertion and removal from a subrack. Specifically, the levers specified here are fully documented in Chapter 8 of the IEEE 1101.10 standard. These levers provide mechanical advantage and positive indexing of the circuit board during insertion and withdrawal. In addition, these units provide the ability to lock the board into the subrack without requiring any tool.

JTAG: Acronym for the IEEE Joint Test Action Group which developed the idea of using dedicated, embedded logic for circuit board testing. This work resulted in the IEEE 1149.1 and subsequent serial test bus standards.

Live Insertion: The ability to insert or withdraw boards while the system is powered and operating without interruption of the system operation or damage to the system.

Monarch: A highly autonomous system element that is responsible for maintaining system order and operation. This element may or may not be implemented on a bus host CPU or System Controller.

Pre-bias: In this context, the application of an analog voltage level to an onboard connector pin prior to its making contact with its corresponding connector pin on an active backplane, to avoid injecting a "glitch".

Pre-leading pin: A VME64x board connector pin which contacts the backplane connector before any of the VME64x signal pins. These early contacts provide a pre-bias voltage to the VME64x board's backplane interface circuitry to ensure glitchless insertion. The 160 pin DIN-style connectors used to accomplish this are specified in IEC 61076-4-113 Detail Specification for Two-Part Connectors Having a Grid of 2.54 mm for Printed Boards and Backplanes.

P1: In this context, the five row by 32 pin VME64x board DIN-style, system bus connector which includes live insertion and high availability support (see ANSI/VITA 1-1994 VME64 Bus Standard).

P2: In this context, the five row by 32 pin VME64x board DIN-style connector which contains the 32 bit VME64 bus extensions, user I/O, and live insertion pre-bias power contacts (see ANSI/VITA 1-1994 VME64 Bus Standard).

SysCon: In this context, the board that contains the VME64x subrack controller function. The SysCon controls bus mastership, interrupt priority resolution and other utility functions. This function is typically included on the bus host CPU board that resides in slot one of the subrack. See ANSI/VITA 1-1994 VME64 Bus Standard.

VME64 compliant: Boards or subrack components compliant with ANSI/VITA 1-1994 VME64 Bus Standard.

VME64x compliant: Boards or subrack components compliant with VITA 1.1-1998 VME64 Extensions Standard.

1.2 References

The following publications are used in conjunction with this standard. When they are superseded by an approved revision, that revision SHALL apply.

Reference #1: *ANSI/VITA 1-1994* VME64 Bus Standard

Reference #2: *VITA 1.1-1998* VME64 Extensions Standard

Reference #3: *VITA 2-199x* Enhanced Transceiver Logic Device Standard, Draft 0.5, August 22, 1997

Reference #4: *IEEE 1101.10-1996* IEEE Standard for Additional Mechanical Specifications for Microcomputers Using the IEEE Std 1101.11-1991 Equipment Practice.

Reference #5: *IEC 61076-4-113* Detail Specification for Two-Part Connectors Having a Grid of 2.54 mm for Printed Boards and Backplanes.

1.3 Standard Terminology

To avoid confusion and to make very clear what the requirements for compliance are, many of the paragraphs in this standard are labeled with keywords that indicate the type of information they contain. The keywords are listed below:

Rule
Recommendation
Suggestion
Permission
Observation

Any text not labeled with one of these keywords describes the VME64x Live Insertion structure or operation. It is written in either a descriptive or a narrative style. These keywords are used as follows:

Rule <chapter>.<number>:
Rules form the basic framework of this draft standard. They are sometimes expressed in text form and sometimes in the form of figures, tables or drawings. All rules shall be followed to ensure compatibility between board and backplane designs. All rules use the "shall" or "shall not" words to emphasize the importance of the rule. The "shall" or "shall not" words are reserved exclusively for stating rules in this draft standard and are not used for any other purpose.

Recommendation <chapter>.<number>:
Wherever a recommendation appears, designers would be wise to take the advice given. Doing otherwise might result in poor performance or awkward problems. Recommendations found in this standard are based on experience and are provided to designers to speed their traversal of the learning curve. All recommendations use the "should" or "should not" words to emphasize the importance of the recommendation. The "should" or "should not" words are reserved exclusively for stating permissions in this draft standard and are not used for any other purpose.

Suggestion <chapter>.<number>:
A suggestion contains advice, which is helpful but not vital. The reader is encouraged to consider the advice before discarding it. Some design decisions that need to be made are difficult until experience has been gained. Suggestions are included to help a designer who has not yet gained this experience.

Permission <chapter>.<number>:
In some cases a rule does not specifically prohibit a certain design approach, but the reader might be left wondering whether that approach might violate the spirit of the rule or whether it might lead to some subtle problem. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. All permissions use the "may" words to emphasize the importance of the permission. The lower-case "may" words are reserved exclusively for stating permissions in this draft standard and are not used for any other purpose.

Observation <chapter>.<number>:
Observations do not offer any specific advice. They usually follow naturally from what has just been discussed. They spell out the implications of certain rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules so that the reader understands why the rule must be followed.

2. Live Insertion Overview

This chapter is informative only. It is provided to give the user the rationale behind the subsequent rules and requirements and exposes the underlying system assumptions used during the development of this standard.

2.1 Application System Objectives

The application systems that use this live insertion capability are typically designed to provide an number of useful services. These may include:

2.1.1 On-line board replacement

Boards that are, or are suspected to be, defective are removed and replaced with a board of similar function. Boards may also be replaced as part of a scheduled maintenance procedure for a revision upgrade. Software orchestrates the orderly reconfiguration of the system upon the removal or replacement of boards.

2.1.2 On-line system expansion

When a system contains insufficient functional capacity, additional boards may be added to the configuration. Software reconfigures system resource pools, and adds the new capacity dynamically.

2.1.3 On-line configuration changes

When a system contains inappropriate amounts of certain board functions, the excess boards may be replaced with other needed board types. Software provides the orderly removal of excess capacity, reconfigures system resource pools, and adds the new capacity to resource pools.

2.2 Live Insertion System Objectives

The objectives in this section examine the individual system needs and influences that permit live insertion to be accomplished at the hardware level.

2.2.1 No damage during insertion/removal

During board withdrawal or insertion no damage should occur to boards or to any connected element of a powered and operating VME64x compliant system.

2.2.2 No mechanical interference

Board dimensions should stay within the overall height requirements of ANSI/VITA 1-1994 VME64 Bus Standard to prevent adjacent board damage. A non-conductive cover prevents incidental contact to adjacent boards during insertion and removal.

2.2.3 Electrostatic discharge (ESD) protection

To avoid system upset as boards contact the backplane connectors, electrostatic energy drain systems are needed on board and chassis elements.

2.2.4 No system upset

A system upset may be the result of corrupted VME64x bus information, lost or spurious interrupts or bus requests, transient upset of bused power sources, or software failing to deal with insertion or removal of boards. The definition of system upset includes the inability of system software to function correctly after boards are added or inadvertently removed without explicit configuration software notification.

2.2.5 Power control

No board power circuits except for pre-bias circuits are active during the live insertion or removal process. Compliant boards isolate all power loads to inhibit arcs at the power contacts on live-system board withdrawal or insertion. Compliant boards also ramp down and up board power to minimize system current transients and power supply overshoot when the system power load is changed as boards are withdrawn or inserted.

2.2.6 Geographic (slot) Address

VME64x boards support the ability to obtain the geographic (slot) address from the P1 connector to locate, in system memory space, the Configuration ROM (CR) (see *ANSI/VITA 1-1994* VME64 Bus Standard and *VITA 1.1-1998* VME64 Extensions Standard) for the purpose of board identification.

2.2.7 Visual status indication

In addition to operational indicators on the board (e.g. running and failed), indicators should be provided to make it clear to a service person that they:

1. Cannot remove the board without causing a system upset.
2. Should not remove the board, but may without causing a system upset (e.g. the configuration software has not been notified of an impending live insertion event).
3. The board is ready for removal.

This may be accomplished with one or more indicators; however, it is standard practice to use as few indicators as possible.

2.2.8 Product identification

All boards that incorporate live insertion capability provide a means to identify their level of Live Insertion capability to the Monarch through the VME configuration ROM (CR).

2.2.9 Live Insertion capable board and backplane connectors

Additional connector pins, which mate before the system bus pins, provide pre-bias power to implement live insertion.

2.2.10 Errant Board Recovery

When an embedded, software-driven board experiences lockup or begins to execute anomalously, a means to recover control and reload the embedded software load is needed. One possible mechanism is a Monarch initiated reset of the board.

2.2.11 Service personnel participation

It is very desirable that all board withdrawal or insertion functions and features be as self completing as possible. The ultimate goal of live insertion system is to only require the maintenance person to physical remove or insert boards into the chassis.

2.3 Overall Live Insertion Process

Note: See Figure 3-1 for circuit diagram.

2.3.1 Insertion Process

1. Board enters the guide rail and contacts the ESD contact in the guide-rail.
2. Static charge on board front panel and Service Person are discharged to FRAME ground through bleed resistor A.
3. Bleed resistor A breaks contact with FRAME ground, board front panel is isolated.
4. Board logic ground is discharged to FRAME ground through bleed resistor B.
5. Bleed resistor B breaks contact with FRAME ground, logic ground is isolated.
6. Board front panel makes low resistance contact with FRAME ground
7. Board connector contacts ground and Vpc (Precharge Voltage) pins on backplane.
8. Bus interface reset signal is generated.
9. VMEbus interface ASICs that are powered by Vpc stabilize and reset.
10. VMEbus signal pins are precharged.
11. VMEbus signal pins and remaining power pins contact the backplane.
12. Ejector handles are seated and handle switches close.
13. Blue LED on board front panel is turned ON.
14. Board waits for LI/I* signal to go low. (LI/I* may be tied low on the backplane or controlled by a centralized device.)
15. Board's power-up sequence continues.
16. Board logic reset signal is generated.
17. BREQ* and INTn* are inhibited.
18. VMEbus interface ASICs and ETL transceivers are enabled. (The circuitry on the board that connects the BG[0:3]* and IACK signal inputs to outputs must remain disabled).

2.3.2 Typical Board Recognition Process

1. Host processor polls the backplane and discovers the new board.
2. Host processor looks at the board's CSR and identifies the board.
3. BIST software is downloaded into the board and run.
4. Embedded software is downloaded into the board and run.
5. Board waits for BG[0:3]* and IACK* on backplane to go inactive and then drives LI/O* low. Daisy-chain switch on backplane is disabled.
6. The circuitry on the board that connects the BG[0:3]* and IACK signal inputs to outputs is enabled. BREQ* and INTn* are enabled.
7. Blue LED on board front panel is turned OFF.
8. Board can now participate in VMEbus transactions.

2.3.3 Typical Board De-allocation Process

1. System administration software disables new connections to board's device driver.
2. System waits for all connections to terminate or forces existing connections to terminate.

2.3.4 Extraction Process

1. Board waits for BG[0:3]* and IACK on backplane to go inactive. BREQ* and INTn* are inhibited. The circuitry on the board that connects the BG[0:3]* and IACK signal inputs to outputs is disabled.
2. Board drives LI/O* high. Daisy-chain switch on backplane is enabled.
3. VMEbus interface ASICs and ETL transceivers are disabled.
4. Board waits for LI/I* to go high or ejector handle switch to open.

5. Service Person grasps ejector handle and is discharged through the front panel to FRAME ground.
6. Service Person unseats the ejector handles and the ejector handle switches open.
7. Board's logic power is removed.
8. Blue LED is turned ON.
9. VMEbus and primary power pins break contact with the backplane.
10. Ground and Vpc pins break contact with the backplane.
11. Board front panel low resistance contact with FRAME ground disconnects.
12. Bleed resistor B makes contact with FRAME ground.
13. Bleed resistor A makes contact with FRAME ground.
14. Board is removed from the guide rail and breaks contact with the ESD contact.

3. Board Design Requirements

3.1 Power Control

It is desirable to have the power control circuits on the product to avoid active circuitry on the backplane and to have any high thermal stress components on the board. This section addresses on-board power control.

3.1.1 Power Switching

RULE 3.1:

On-board circuitry SHALL be disconnected from the VME backplane power pins at the time of board insertion and removal, with the exception of the circuits powered by pre-bias +5 Volt power.

3.1.2 Power Ramp Rate

RULE 3.2:

Power control circuitry SHALL apply or remove power to the board circuitry at a rate not to exceed 2 Amps per millisecond.

3.1.3 Power Control Loss

RULE 3.3:

The power control circuitry SHALL NOT reduce on-board voltages by more than 2% or 100 mV, whichever is more.

3.1.4 Manual Power Control

RECOMMENDATION 3.1:

Locking injector/ejector position sensing handles (see *IEEE 1101.10-1996* IEEE Standard for Additional Mechanical Specifications for Microcomputers Using the IEEE Std 1101.11-1991 Equipment Practice., Chapter 8) SHOULD be included in the board design.

RULE 3.4:

The position sensing injector/extractor handles, if provided, SHALL trigger all board insertion and removal processes.

RULE 3.5:

As a minimum, boards SHALL provide a prominent indicator to warn the service personnel not to remove the board if power is still applied.

OBSERVATION 3.1:

If a power control toggle switch directly switches power to the board circuitry excessive dV/dT and dI/dT will result.

RULE 3.6:

Boards that use a toggle switch to control board power SHALL NOT incur system or board damage if the board is removed or inserted with the switch in the “ON” position.

RULE 3.7:

For boards that use a toggle switch, the "up" switch position, viewed as the board is installed, SHALL select the board “ON” or powered state and the "down" position SHALL select the “OFF” or unpowered state.

3.1.5 Remote Power Control

Due to CMOS latch-up and other soft but unresettable board failure conditions a VME64x LI board might not respond to a power down command. To recover from such a failure condition a mechanism is needed to permit the host to power down the board.

The LI/I* is an active low input signal to a VME64x LI board that enables/disables the on-board power control logic.

Permission 3.1:

The LI/I* can be either floating or driven low by a backplane signal. This signal can be driven by a radial power control module or the slot's transition module.

RULE 3.8:

When the LI/I* signal from P1 (see *VITA 1.1-1998* VME64 Extensions Standard, table 3-1) is driven high the board SHALL immediately disable the on-board power control logic.

RULE 3.9:

The LI/I* signal SHALL be a negative true, open collector driven signal. Its driver SHALL be capable of sinking 8 mA while maintaining a DC signal level no greater than 0.4 V.

RULE 3.10:

The LI/I* signal SHALL be pulled up by resistor on the board connected to pre-bias power. The pull-up resistor SHALL be a minimum of 3.3 KOhm.

Recommendation 3.2:

A 10 KOhm LI/I* pull-up resistor is recommended.

Observation 3.2:

If a VME64xLI board is inserted into a backplane that does not control the LI/I* signal the boards's own sequencing/handle sensor enables the power up. If the LI/I* backplane signal is low, the board stays unpowered after locking and until LI/I* is allowed to go high by the host.

3.1.6 Precharge Power

RULE 3.11:

The total of all pre-bias powered circuits on a board SHALL NOT consume more than 150 mA of current.

3.2 VME64x Bus Interface

3.2.1 VME64x bus signal pre-bias voltage

For P1 and P2 voltage and signal pin reference see VITA 1.1-1998 VME64 Extensions Standard, *Table 3-1.*

RULE 3.12:

All VME system bus drivers and receivers SHALL be pre-biased to +1.7 +/-0.2 Vdc. with a resistive network powered by the pre-bias +5V power (see *VITA 1.1-1998* VME64 Extensions Standard, Table 3-1: Vpc) before the board signal pins contact the backplane VME64x bus connector(s).

Observation 3.3:

IBM has submitted this method of live insertion bus glitch avoidance for patent.

Recommendation 3.3:

The Enhanced Transceiver Logic data bus transceivers (ABTE family) available from T.I. and National include patent license and are recommended.

RULE 3.13:

The pre-bias voltage SHALL be applied to every on-board bus signal that connects to the VME64x system bus on backplane.

RULE 3.14:

On boards with a P1 and P2 connector the pre-bias networks SHALL obtain voltage and ground via the P1-(d)1 and P2-(d)32 pre-bias voltage and P1-(d)2 and P2-(d)31 ground pins (see *VITA 1.1-1998* VME64 Extensions Standard) which receive voltage before the remaining P1 and P2 pins make backplane contact.

RULE 3.15:

On boards with only a P1 connector the pre-bias networks SHALL obtain voltage and ground via the P1-(d)1 and P1-(d)32 pre-bias voltage and P1-(d)2 and P1-(d)31 ground pins(see *VITA 1.1-1998* VME64 Extensions Standard) which receive voltage before the remaining P1 pins make backplane contact.

RULE 3.16:

The precharge network SHALL present a minimum Thevenin equivalent DC resistance of 50 KOhms at each VME64x bus pin.

RULE 3.17:

When and after the LI/O* signal becomes OPEN (see Section 3.3), the VME64x bus signals IACKout* and BG[0:3]* SHALL assume a high impedance state.

3.2.2 Signal Characteristics

RULE 3.18:

The board SHALL provide an LI/O* signal to P1 (see ANSI/VITA 1-1994 VME64 Bus Standard, table 3-1) to indicate to the backplane when it is capable of controlling the backplane daisy chain signals IACK* and BG[0:3]*.

RULE 3.19:

The LI/O* signal SHALL be a negative true, open collector driven signal. Its driver SHALL be capable of sinking 8 mA while maintaining a DC signal level no greater than 0.4 V.

RULE 3.20:

The LI/O* signal SHALL be driven LOW when the board is capable of appropriately handling the IACK* and BG[0:3]* signals as per *ANSI/VITA 1-1994* VME64 Bus Standard, section 4.2 and Section 3.2, respectively.

RULE 3.21:

The state of the LI/O* signal SHALL only be changed when the IACK* and BG[0:3]* signals are inactive.

RULE 3.22:

Whenever the power monitoring circuits indicate that board power is not within tolerance signal LI/O* SHALL be OPEN.

RULE 3.23:

Signal LI/O* SHALL be OPEN when the board is notified of impending removal by either the injector/ejector handle, power switch or via the host software.

Observation 3.4:

Connecting the input and output of a gate together is not a good practice. The backplane daisy-chain module and the board are both capable of managing the IACK* and BG[0:3]* signals. The onboard transceivers that drive the IACK* and BG[0:3]* signals, the onboard circuitry that controls the BREQ* and INTn signals, and the backplane daisy-chain module SHOULD NOT be enabled at the same time.

3.2.3 Host Initiated Reset

Host initiated reset is needed to assure an orderly shutdown of board processes and board removal preparation under all conditions.

RULE 3.24:

System component boards SHALL be provided with at least one means, from the system host CPU, to reset all VME64x bus interface logic and to set I/O drivers into a latched inactive and high impedance (tri-state) condition.

RULE 3.25:

System component boards SHALL be provided with at least one means, from the system host CPU to put all processors on the board into a latched reset state.

3.3 Power Off Interrupt

RULE 3.26:

A special interrupt type or vector SHALL be generated to the host CPU when a power off sequence is initiated, either by the injector/extractor handle sensor or by a toggle switch.

3.4 Host Notification

When a board is about to be removed, a high priority interrupt is needed to notify the host in the event the host did not request the removal. When a board has been inserted it responds to polling with its slot number.

RECOMMENDATION 3.4:

A dedicated interrupt (INT*n*) register or manual selection device SHOULD be provided on each board to generate a high-priority interrupt, which is used only when notifying the host of impending removal of the board.

RULE 3.27:

After a board has been inserted and powered up but is still in reset, it SHALL respond to any VMEbus READ access within it's slot-selected A24 bus address with it's 8 bit binary slot number, i.e.: slot 10 = 00001010b. The slot-selected A24 bus address = <slot #> X 512K (80000H).

3.5 Mechanical Requirements

RULE 3.28:

6U live insertable boards SHALL comply with ANSI/VITA 1-1994 VME64 Bus Standard, section 2.2.1, 6U VME64x Board's Minimum Features. 3U live insertable boards SHALL comply with ANSI/VITA 1-1994 VME64 Bus Standard, section 2.2.2, 3U VME64x Board's Minimum Features. These requirements include the special 5-row 160 pin IEC 1076-4-1xxx connector.

3.5.1 Visual Indicators

RULE 3.29:

A red LED "FAIL/INACTIVE" SHALL provide visual indication that a board has been reset, powered down and is ready for removal.

RULE 3.30:

A green LED "RUNNING" indicator SHALL provide visual indication that any on-board control processor is executing normally.

RECOMMENDATION 3.5:

For any other powered board state, i.e.: loading, testing, detectable anomalous (i.e.: watchdog time-out) operation, etc., both the FAIL and RUNNING lights SHOULD be lit.

3.5.2 ESD Drain Contact

RULE 3.31:

A printed wiring strip for draining ESD energy during board live insertion SHALL be provided. The recommended ESD drain contact system is described in IEEE 1101.10-1996 IEEE Standard for Additional Mechanical Specifications for Microcomputers Using the IEEE Std 1101.11-1991 Equipment Practice, chapter 9, figure 17. The strip SHALL be segmented as illustrated in figure 3-1 and figure 3-2.

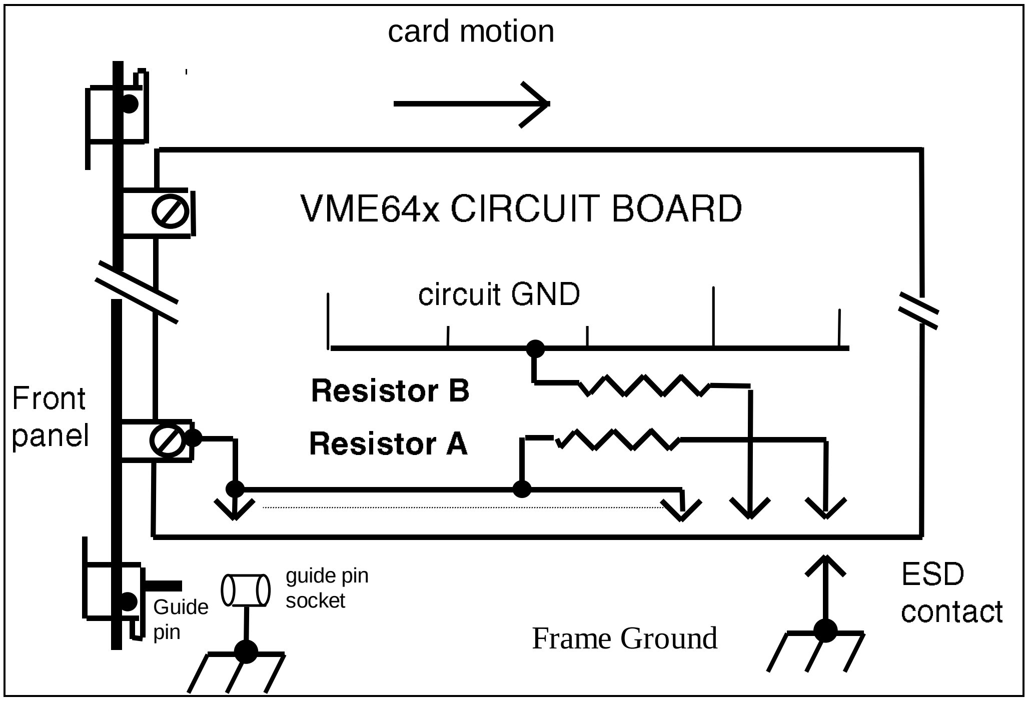

Figure 3-1. ESD Drain Contact Arrangement

RULE 3.32:

The board SHALL have galvanically isolated electrostatic energy discharge paths from the front panel and from the DC circuits to the ESD discharge strip per figures 3-1 and 3-2.

RULE 3.33:

The initial ESD current from the front panel or DC circuits SHALL be limited by a minimum of 2 resistors in series with a total breakdown voltage of 800 Volts. The total discharge current limiting resistance for each discharge path SHOULD be 2 to 10 MegOhms (see Resistor A and Resistor B in figure 1).

RULE 3.34:

The front panel and DC circuits SHALL be discharged within the first 35 mm. of board insertion into the rack (see figure 2). The board grounding contacts SHALL be arranged so as to prevent the chassis contact from bridging the two contacts and possibly causing front panel ESD to discharge into the board DC circuitry.

RULE 3.35:

There SHALL be 15 mm. nominal space between the front panel and DC ground discharge contacts to prevent simultaneous contact and possibly transferring charge from the front panel to the circuitry (see figure 2).

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RULE 3.36:

The front panel discharge path SHALL be in contact with the chassis discharge contact for most of the insertion travel of the board to continuously drain ESD generated by the service person's motion (see figure 2).

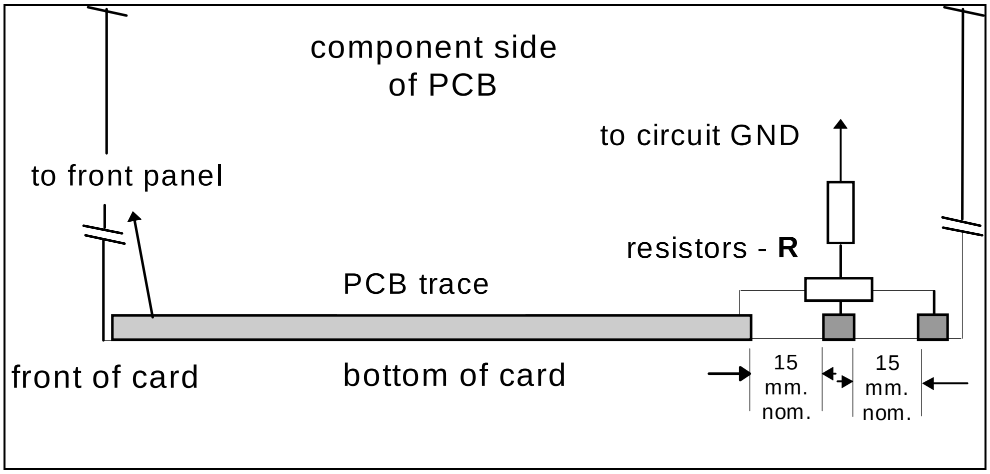

Figure 3-2. ESD Contact Strip Details

RULE 3.37:

The faceplate guide pin receptacle SHALL provide a low impedance path to chassis (safety) ground capable of carrying a 25 Ampere fault current.

3.5.3 Backplane Connectors

The 5-row, 160 pin IEC 1076-4-1xxx connectors provide the staged length contacts and additional pin functions that permit live insertion.

RULE 3.38:

The 5-row, 160 pin IEC 1076-4-1xxx connectors for P1 and P2 (if 6U board) SHALL be used in compliance with ANSI/VITA 1-1994 VME64 Bus Standard, chapter 3.

3.5.4 Injector/Extractor Motion Sensing Handles

Injector/extractor handles ease insertion and extraction. Some versions have sensing switches that detect when extraction motion has just begun and signal when a board is fully seated. Both board top and bottom sensing switches reliably coordinate removal and insertion operations.

RECOMMENDATION 3.6:

The injection/extraction handles complying with IEEE 1101.10-1996 IEEE Standard for Additional Mechanical Specifications for Microcomputers Using the IEEE Std 1101.11-1991 Equipment Practice, chapter 8 and equipped with top and bottom sensing switches SHOULD be used to provide the best possible system availability by providing a non-cooperative service person interface that senses motion.

3.5.5 Board Keying

This standard and other VME enhancements are targeted specifically at highly available and maintainable systems. Preventing the insertion of wrong board types into specific system slots is integral to service-tolerant maintainability. The use of an alignment pin in conjunction with keying provides the most robust blocking of invalid keying codes.

RECOMMENDATION 3.7:

Keyed faceplates that include an alignment pin as specified by IEEE 1101.10-1996 IEEE Standard for Additional Mechanical Specifications for Microcomputers Using the IEEE Std 1101.11-1991 Equipment Practice, chapter 6 SHOULD be provided.

3.5.6 Solder-Side Dielectric Covers

VME board spacing and tolerances do not guarantee non-interference during live system maintenance. Incidental contact with adjacent boards during board insertion and removal can disrupt the operation of the victim board. Since the most likely surface for this incidental contact is the inserted/removed board solder-side, an appropriate dielectric cover can prevent this event.

RECOMMENDATION 3.8:

A solder-side, dielectric cover SHOULD be provided as specified by IEEE 1101.10-1996 IEEE Standard for Additional Mechanical Specifications for Microcomputers Using the IEEE Std 1101.11-1991 Equipment Practice, chapter 7.

4. Subrack (shelf) Requirements

4.1 Backplane Requirements

The following requirements refer to the printed wiring board that supports the J1 and J2 daughterboard connectors, which provide system busing, interrupts and bus grant daisy chains, power distribution, etc.

4.1.1 Daughterboard Connectors

RULE 4.1:

Backplanes SHALL use for P1 and P2 (if 6U board) daughterboard connectors the 5-row 160 pin IEC 1076-4-1xxx connectors specified VITA 1.1-1998 VME64 Extensions Standard, section 3.2.

4.1.2 Precharge Power

The J1 and J2 (if 6U board) 160 pin connectors have pins assigned for pre-bias +5 Volts and ground.

RULE 4.2:

On 6U board slots the backplane SHALL provide pre-bias +5 Volts and ground via J1 and J2 pre-bias voltage pins J1-(d)1 and J2-(d)32 and ground pins J1-(d)2 and J2-(d)31 (see ANSI/VITA 1-1994 VME64 Bus Standard, section 3.2.6) which apply voltage and ground before the remaining P1 and P2 pins make board contact.

RULE 4.3:

On 3U board slots the backplane SHALL provide pre-bias +5 Volts and ground via pre-bias voltage pins J1-(d)1 and J1-(d)32 and ground pins J1-(d)2 and J1-(d)31 (see ANSI/VITA 1-1994 VME64 Bus Standard, section 3.2.6) which apply voltage before the remaining P1 pins make board contact.

4.1.3 Geographic Addressing

The ability to provide a physical slot identification code to live insertable boards is required to provide adequate system configuration control and to support high availability functions.

RULE 4.4:

Backplanes SHALL provide J1 geographic addresses for all live insertable board slots as per ANSI/VITA 1-1994 VME64 Bus Standard, section 3.2.

4.1.4 Bus Grant and Interrupt Priority Arbitration

VME backplanes have four daisy-chained Bus Grant (BG*n**) signals and one daisy-chained Interrupt Acknowledge (IACK*) signal that perform bus and interrupt arbitration. For additional details see ANSI/VITA 1-1994 VME64 Bus Standard, chapters 3 and 4, respectively. Early designs of VME backplanes included installable jumpers to bypass empty backplane slots and thus maintain the continuity of the daisy-chain signals. Later designs of backplanes included electronic bypass jumpering built into the backplane. The electronic jumpering versions typically sense the presence of a VME board **during power-up of the VME system** and connect the daisy-chains accordingly. Mechanical switches were later added to backplane connectors providing the same jumper-less configuration without any electronics. None of these electronic or mechanical implementations will support Live Insertion.

The live insertion process depends on the backplane to provide mechanisms to allow the daisy chained bus grant arbitration and interrupt priority resolution processes to continue unaffected during live insertion or removal. There are two recommended methods to accomplish this, with centralized (or radial) arbitration done by a dedicated system board or with daisy-chain bypass circuits mounted on the backplane.

The VITA proposed centralized arbitration scheme provides excellent flexibility and increased system performance in exchange for higher backplane and subrack cost and complexity. This arbitration scheme is described in the *VITA 1.x-199x High Availability VME* draft standard and is beyond the scope of this document.
The backplane mounted daisy chain bypass circuits described here provide a low cost, highly configurable solution. To provide acceptable backplane serviceability and configurability the daisy chain bypass circuits are best implemented as per-slot, removable modules. Designing to the mechanical module format described here will ensure the widest industry availability.

4.2 Daisy Chain Switch Module

All of the electrical functions required for VME64x Live Insertion can be placed on the VME64x function board except for the backplane daisy-chain bypass circuits. Since these bypass circuits must replace the withdrawn board, the bypass circuits must be located on the backplane or in a CSM or SysCon module.
The following describes a standardized backplane daisy-chain module format.

4.2.1 Daisy-Chain Module Behavior

The following sections describe only the functional requirements of the bypass module to leave room for improvements in the technology used. The electrical portions must comply with chapters 3 and 4 of ANSI/VITA 1-1994 VME64 Bus Standard, as appropriate.

RULE 4.1:

The LI/O* signal (see section 3.2.2) SHALL be used for controlling the action of backplane daisy-chain module and SHALL function as follows:

(1) When the LI/O* signal for a given VME64x backplane slot is at a logic HIGH level:

-The interrupt priority signals IACKin* and IACKout* SHALL be electrically connected together.

-The BG[0:3]in and BG[0:3]out SHALL, individually, be electrically connected, input to output.

(2) When the LI/O* signal for a given VME64x backplane slot is at a LOW logic level the IACK* and BG[0:3] daisy-chain signals SHALL NOT be connected across the VME board slot by the daisy-chain module.

OBSERVATION 4.1:

If a non-VME64x compliant board is installed into a VME64x backplane slot having the bypass module installed, the VME board will not be able to participate in the VME64 interrupt priority or bus arbitration processes.

RECOMMENDATION 4.1:

VME64x boards that do not support Live Insertion SHOULD tie the LI/O* pin to ground. If a given slot is equipped with the daisy-chain module, The LOW logic level on LI/O* will cause the module to turn off, giving the VME64x board control of that slot's daisy-chain signals.

RULE 4.2:

The daisy-chain module SHALL comply with the electrical specifications described in of ANSI/VITA 1-1994 VME64 Bus Standard, chapter 4 concerning IACK* and BG[0:3]* signals.

PERMISSION 4.1:

The VME64x backplane may be designed with all of the daisy-chain modules incorporated into a centralized location (CSM). The centralized resource must comply with RULE 4.1.

4.2.2 Implementation of the Backplane daisy-chain module

This section describes a recommended backplane pin arrangement to allow a small module to be mounted perpendicular to the backplane on the rear side between each board slot connector . See figure 4-1 for the module illustration.

OBSERVATION 4.2:

In order to reduce system implementation cost and increase compatibility between vendors, plug-on daisy-chain modules SHOULD have the same mechanical, electrical, and behavioral characteristics. This will allow any vendor's daisy-chain module to work with any vendor's backplane and VME64x board. This will not prohibit a backplane vendor or integrator from using a particular technology to implement a daisy-chain module.

RECOMMENDATION 4.2:

VME64x backplanes SHOULD have the BG[0:3] and IACK* signals connected to a row of standard 0.025” wire-wrap pins. The wire-wrap pins SHOULD be 17 mm long and be arranged according to Table 4-1. The connections to the bypass module for the +5V, LI/O*, and GND connections SHOULD be standard 0.025” wire-wrap pins.

Signal	Pin Number	Format	† Relative Dimension
BG0OUT*	1	PIN	0.0”
BG0IN*	2	PIN	0.1”
BG1OUT*	3	PIN	0.2”
BG1IN*	4	PIN	0.3”
BG2OUT*	5	PIN	0.4”
BG2IN*	6	PIN	0.5”
BG3OUT*	7	PIN	0.6”
BG3IN*	8	PIN	0.7”
+5V	9	Socket	1.1”
LI/O*	10	Socket	1.2”
GND	11	Socket	1.3”
IACKIN*	12	PIN	1.7”
IACKOUT*	13	PIN	1.8”

† = distance down from the first (top) pin of the array.

Table 4-1. Daisy Chain Module Pinout

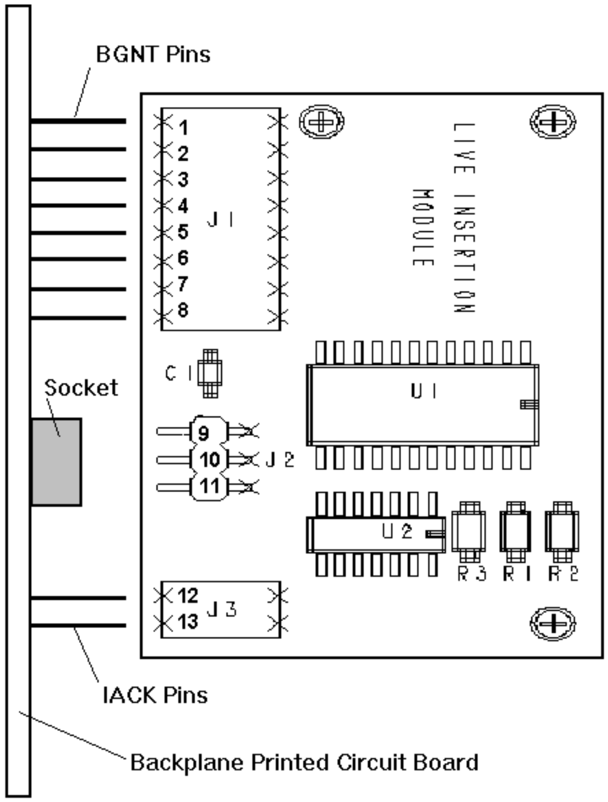

Figure 4-1. Recommended Daisy Chain Module Layout

RULE 4.3:

The daisy-chain module SHALL have a pull-up resistor of 4.7 KOhm nominal on the LI/O* signal to insure that the signal is at a high level when a VME64x board is not installed in a backplane slot.

4.3 Plug-in Board (VME64x board) Connectors

The J1 and J2 mating board connectors on the backplane SHALL comply VITA 1.1-1998 VME64 Extensions Standard, chapter 3.

4.4 Chassis Requirements.

4.4.1 Injector/Extractor Handle Support

RULE 4.4:

The subrack top and bottom sheet metal SHALL provide appropriate mating cutouts for the engagement tab of the injector/extractor front panel handles in compliance with IEEE 1101.10-1996 IEEE Standard for Additional Mechanical Specifications for Microcomputers Using the IEEE Std 1101.11-1991 Equipment Practice, section 8.1.

4.4.2 Board Keying Support

As addressed in section 3.5.5, support is needed to prevent inappropriate boards from being plugged into VME64x board slots. IEEE 1101.10-1996 IEEE Standard for Additional Mechanical Specifications for Microcomputers Using the IEEE Std 1101.11-1991 Equipment Practice includes a board guide with keying that mates with compliant and appropriately keyed front panels. A receptacle for the accompanying alignment pin is essential to robust keying.

RULE 4.5:

Chassis board guides that support keying with alignment pin support per IEEE 1101.10-1996 IEEE Standard for Additional Mechanical Specifications for Microcomputers Using the IEEE Std 1101.11-1991 Equipment Practice, chapter 6 SHALL be provided.

4.4.3 Board Guide ESD Drain Contact

To drain accumulated electrostatic potential from an inserted board, a grounded board guide contact clip is needed which mates with the board drain strip specified by section 3.5.2.

RULE 4.6:

A chassis board guide ESD drain contact SHALL be provided as specified by IEEE 1101.10-1996 IEEE Standard for Additional Mechanical Specifications for Microcomputers Using the IEEE Std 1101.11-1991 Equipment Practice, chapter 9.

4.4.4 Front Panel Safety Grounding Support

For personnel protection, telecom systems are required to provide a low resistance path from all external conductive surfaces to the system grounding point. The front panel guide pin specified by IEEE 1101.10-1996 IEEE Standard for Additional Mechanical Specifications for Microcomputers Using the IEEE Std 1101.11-1991 Equipment Practice, chapter 6 for mechanical board indexing can also provide a low resistance path from the faceplate to the chassis sheet metal for power fault protection. A guide pin mating contact galvanically connected to the subrack sheet metal is needed to complete this ground path.

RECOMMENDATION 4.2:

A low resistance, front panel guide pin grounding contact SHOULD be provided on the chassis sheet metal supporting the board guides. If provided, the path resistance measured from the faceplate to the subrack sheet metal SHALL NOT exceed 40 milliOhms.

5. Host System Requirements

5.1 Bus Error (catch) Module

Live insertable systems need coverage for all conditions that may arise during the board insertion or removal operation for the system to be viable. If an attempt is made by the bus to access a board after it has been electrically or physically disconnected from the system, a bus error will result (see ANSI/VITA 1-1994 VME64 Bus Standard, section 2.2.4.4). High availability systems must avoid bus errors since these typically result in one of a variety of non-recoverable bus host error states.

When the service person activates the injector/ejector handle switch the board is removed from the system's resource list, the board's drivers finish handling queued operations, the board's drivers are disabled, and the board is disconnected from the bus. Even though the board is installed in the chassis, the board cannot be accessed through the VMEbus. If the host tries to access the now disconnected board an excessive length bus access cycle will occurr. In most VMEbus systems the host will report this as a bus error. In VMEbus High Availability systems a bus error trap or "catch" module detects the excessive length bus access cycle and then intervenes to complete the bus cycle, thereby avoiding a host-detected bus error. This catch module can also capture the bus address of the offending bus cycle and provide this recovery information to an appropriately designed host software module.

The physical packaging of this module is left to the VME product vendors. However, this module has standardized VMEbus mapping so that any vendor's catch module is identically accessed.

5.1.1 Bus timer

A programmable bus timer is needed to detect a bus fault. This timer must be shorter than any default bus host bus timer.

RULE 5.1:

A bus fault SHALL be declared whenever the VME64 bus signal AS* is active for more than a preset time period with a DTACK* signal being returned by a slave board.

RULE 5.2:

The bus fault timer SHALL offer a preset period of 5 to 10 microseconds, as a default minimum.

5.1.2 Address capture

The module needs to capture a significant portion of the A24, A32 or A64 bus address.

RULE 5.3:

The bus error (catch) module SHALL, as a minimum, capture the following VMEbus addresses:

(1) A24 accesses: address bits A16 through A23.
(2) A32 accesses: address bits A24 through A31.
(3) The address modifier code (AMC)

RECOMMENDATION 5.1:

The capture register SHOULD be implemented 32 bits wide and the extended modifier code (XAM) be appended to the AMC.

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RULE 5.4:

The address modifier codes SHALL be captured and right justified within the byte.

5.1.3 Interrupt Generation

When the catch module captures a bus fault, a high priority interrupt to the bus host is generated.

RULE 5.5:

The module SHALL be capable of generating any bus interrupt 1-7.

PERMISSION 5.1:

The module MAY permit VMEbus INT1-7 selection via manual jumpers or be software programmable.

RULE 5.6:

An 8 bit interrupt vector shall be generated in response to the VMEbus interrupt acknowledge cycle.

PERMISSION 5.2:

The vector specified in Rule 5.6 MAY be settable via switches or by software.

RULE 5.7:

Subsequent bus faults SHALL be ignored until the host interrupt has been acknowledged and the capture register has been read.

OBSERVATION 5.1:

If the interrupt generated by the bus error (catch) module is not acknowledged before the next bus fault a non-recoverable error will occur.

RULE 5.8:

Once the address capture register has been read it SHALL be cleared by the catch module, and the capture mode re-armed.

5.1.4 VME64 Bus Mapping

The bus error (catch) module SHALL provide the following

Bus Address	Byte 0	Byte 1	Byte 2	Byte 3
xxFFFF00H (READ)	AMC (xxxbbbbb)	XAM (bbbbbbbb)	capture register	reserved
xxFFFF00H (WRITE)	INT number (bit mapped)	INT vector (optional)	Timeout value (optional)	

Table 7-1. Catch Module Register map

5.1.5 Bus Fault Interrupt Service Module

An interrupt service module is needed to support the catch module. See section 7.x.

6. I/O Considerations for Live Insertion (For Information Only)

Not only the system bus is affected by the live insertion of boards into a functioning system but all the I/O connections to that board as well. This section covers general suggestions for live insert tolerant I/O.

6.1 Discrete I/O

Open drain/collector drivers
Pulled up on transition module
Q-switches on transition module
Overvoltage clamping
Serial bus

6.2 P2 Subbuses

ASIC live Insertion output pads
“Float” Interface chip
Q-switches

7. Host Application Utility Software

The software supplied with a live insertable board will determine its usability. This section highlights special considerations inherent in systems that allow boards to be removed and inserted while "hot".

7.1 Mandatory Operations Software

RULE 7.1:

The following set of software functions SHALL be provided in some form to adequately support VME64x board live insertion and removal system functions.

7.1.1 Callable Loader

If a VME64x board has processors, the host will typically need to download executable code and configuration files to the board before it can operate. A loader is the generic name for a utility program that can communicate with the uninitialized board, access the executable and configuration files, (whether disk or network based), load the board and then leave it in a state where it can be accessed by the host board's driver.

RULE 7.1:

The loader SHALL be callable from the application program or USER partition.

RULE 7.2:

The loader SHALL provide the following minimum functions after the live insertion of a VME64x board:

(1) Receive and handle the "new board" interrupt vector.
(2) Initiate configuration of the new board.
(3) Command the board to power up, if necessary.
(4) Download a boot-up diagnostic and the Build In Self Test (BIST) (either via VME64 bus commands or via the H.A.VME Utility Communications Channel) and report the results to the application.
(5) If BIST completes successfully, command the VME64x board to enable it's VMEbus transceivers, if appropriate,
(6) Download the operating software (including checksum verification, if necessary), and start program execution.
(7) Establish a dialog with the operating software and download any additional configuration information to the board. Then return notice of a successful insertion to the application program.

7.1.2 Configurable Driver

The driver software is the interface between the application program and the VME64 board physical VMEbus interface. There are several areas of concern for a successful live insertion driver:

RULE 7.3:

The driver needs to provide an "administration" interface to allow the application to query and change the number of boards which are registered and available to the application program.

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RULE 7.4:

The driver needs to gracefully handle application requests for non-existent boards or functions.

RULE 7.5:

The driver interface to the board needs to be tolerant of all failures of communication with the board and return meaningful error codes to the application program.

RECOMMENDATION 7.1:

The driver SHOULD provide a "watchdog" function to detect silent board "death".

PERMISSION 7.1:

The driver may either poll or detect an interrupt from newly inserted boards.

RULE 7.6:

The driver SHALL NOT, under any anticipated or recoverable operation, cause a catastrophic or non-recoverable system event like a UNIX "kernel panic".

RULE 7.7:

The driver SHALL provide an interface to the "catch" module driver and provide functionality to abort activities to reported non-responsive boards and then report the loss, via meaningful error codes, to the application program.

7.1.3 "Catch" Module Driver

The catch module driver needs to run at the kernel or system level and at a higher priority than the associated drivers so as to intercept in-process commands that have failed due to a board being preemptively removed or becoming non-responsive.

The driver needs to access the driver's board address tables to determine which logical resource unit corresponds with the captured bus address returned by the catch module.

The driver needs to communicate with the function driver to notify it that a board resource is no longer responding.

7.1.4 New Board Poll Routine

A host software module is needed which continuously "looks" for just-inserted boards.
This software module operates in concert with the catch module driver to poll (READ) from one address in each currently vacant 512K address segment for boards which have been just inserted.
If no board is found at the vacant address the catch module will capture and return the high order 8 bits of the bus address read from.
If a board has been just inserted and is ready to be configured it will, itself, respond to the poll with its slot number which should match the poll address.
The poll module returns the slot number to the application software to begin the download process.

7.2 Optional Software

7.2.1 Configuration Utility

A system configuration utility allows adjustments to be made in the type or number of VME function boards installed and available in a given VME64x system.
The most reliable system administration and maintenance is provided when the application software notifies the VME64 board driver subsystem, *a priori*, that changes involving changing the number and type of installed boards are to be made in the system configuration.

Both the catch module service and new board poll routines should be part of this utility package so that newly inserted boards can be automatically be recognized and even autoloaded and configured as they are inserted, if desired.

The configuration utility should have both an interactive (console) and remote interface options to allow an operator to query and adjust the system configuration tables on-line.

The configuration utility should also provide board power control, if boards are so equipped.

The configuration utility should be capable of handling any vendors' boards so standardized board type file structures are needed. The type structures list acceptable board type (CR) codes and associated executable code filenames and any other parameters required for initialization.

Highly functional configuration utilities typically provide an SNMP or CMIP proxy interface to provide for networked system management support.

7.2.2 Off-Line Diagnostic Utility

Off-line diagnostic programs provide the ability to exhaustively test newly inserted boards or to exercise boards that have been removed from active service to validate suspected faults.

The diagnostic should have an interactive and remote interface to allow local or remote maintenance operations.

The diagnostic should not interfere with any other live system functions or operations other than consuming some system bandwidth.

The diagnostic should be driven by a table of board diagnostic downloadables and test script options. The table structure, global test options and gross return codes should be standardized.