

PMC-P4 Pin Out Mapping To VME-P0 and VME64x-P2 Draft Standard

VITA 35-199x

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VITA Standards Organization
7825 East Gelding Drive, Suite 104
Scottsdale, AZ 85260
Ph: 480-951-8866 Fx: 480-951-0720
URL: <http://www.vita.com>

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Task Group Members

Sponsors

Jing Kwok	DY 4 Systems Inc	jkwok@dy4.com
Alan Storrow	Radstone Technologies PLC	storrow@radstone.co.uk
Doug Patterson	SBS Embedded Computers	dpatterson@sbs-ec.com
Gorky Chin	VISTA Controls Corporation	gorky@vistacontrols.com

Participants and Observers

Scott Annis	Winchester Electronics	s.annis@litton-wed.com
Stephen Cecil	NSWC Crane Division	cecil-s@crane.navy.mil
Douglas Endo	Raytheon System Company	dendo@west.raytheon.com
Frank Hom	APW Electronic Solutions	fhom@apw-elsol.com
Robert McKee	MITRE Corporation	rmckee@mitre.org
Gregory Novak	Motorola Computer Group	greg@phx.mcd.mot.com
Elwood Parsons	AMP Incorporated	etparson@amp.com
Mac Rush	Motorola Computer Group	rush@phx.mcd.mot.com
John Rynearson	VITA	techdir@vita.com
Holly Sherfinski	Harting Inc. of North America	holly.sherfinski@harting.com
Mark Taylor	Bechtel Bettis Inc	taylormg@bettis.gov
Mike Macpherson	VISTA Controls Corporation	mac@vistacontrols.com

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0.3	June 30, 1999	Fixed errors in P4V2-32+32ac
0.4	September 19, 1999	Incorporate Working Group Review Comments from July 22, 1999 VSO meeting

Comments, Corrections and/or Additions

Anyone wishing to provide comments, corrections and/or additions to this proposed draft standard, please direct them to the Task Group chair:

Jing Kwok, VITA 35-199x Chair & Draft Editor
DY 4 Systems Inc. 333 Palladium Dr
Kanata, Ontario, Canada K2V-1A6
Phone: 613-599-9199 Fax: 613-599-7777
Email: jkwok@dy4.com Web site: <http://dy4.com>

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Chapter 1

Overview

1.1. Overview

This standard defines the mapping for the pinout between a PCI mezzanine Card (PMC) module's user IO connector (P4) and the VME host's user IO connector. Four mappings are defined in this document.

Other standards such as Compact PCI (CPCI) which supports a PMC and a VME-P0 style connector on the host could also use this standard.

Figure 1 shows a diagram of the components referenced in this standard.

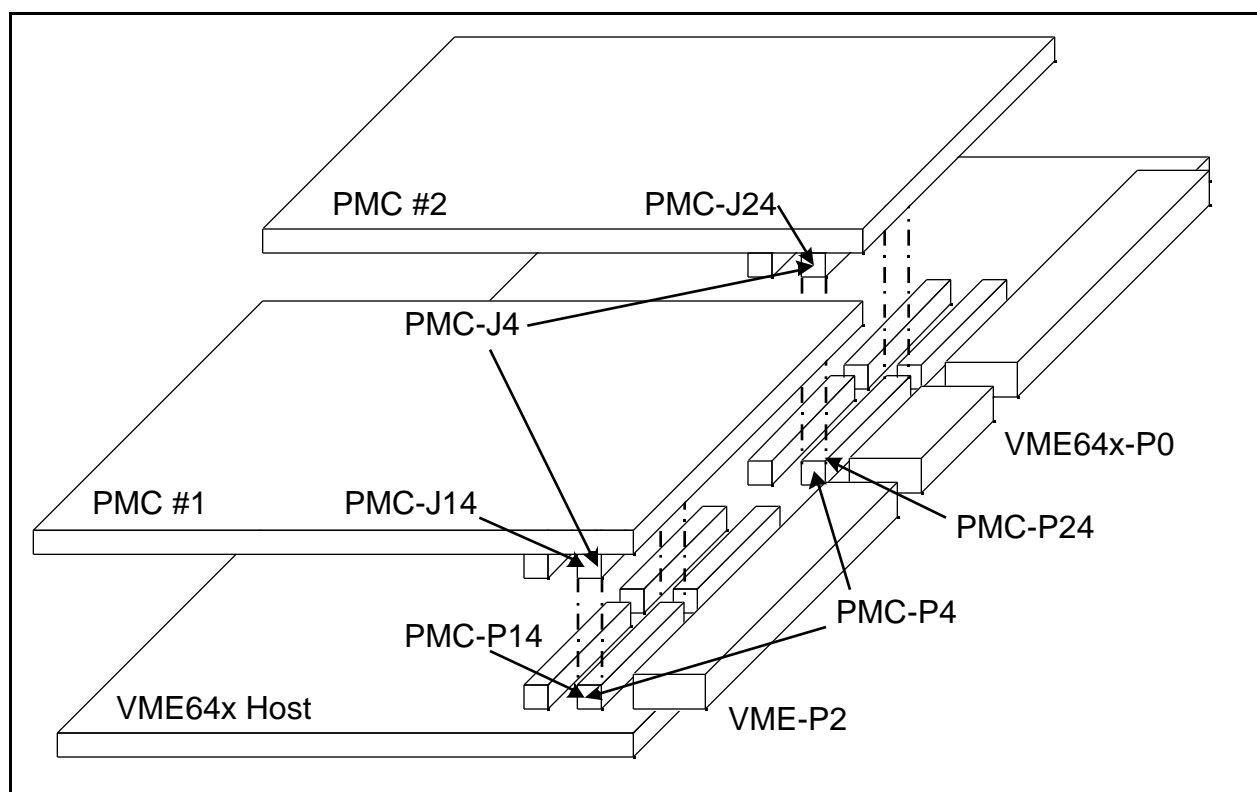


Figure 1 : PMC on VME Host

1.2 References

IEEE P1386-199x CMC Draft Standard April 4, 1995
CMC/P1386, Draft 2.0 - Major Text Edits October 14, 1997
Connectors : IEC 60603-2, IEC 61076-4-101, IEC 61076-113

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1.3 Acronyms, Abbreviations, Definitions and Terminology

The following abbreviations are utilized throughout this document and are stated here for clarification.

CMC	Common Mezzanine Card. This is the mechanical standard for a PMC module. This is also known as IEEE P1386.
CPCI	Compact PCI. This is a mechanical and electrical standard used to interconnect rack mounted board level product. The electrical specifications are based on PCI and the mechanical specifications resemble a VMEbus card using 2mm connectors.
PCI	Peripheral Chip Interconnect. This is an electrical standard designed to interconnect devices at a chip and board level.
PMC	PCI Mezzanine Card. This is the electrical standard for a CMC module. This is also known as IEEE P1386.1.
VME	Versa Module Eurocard. This is used interchangeably with VMEbus. This is a mechanical and electrical standard used to interconnect rack mounted board level product.
VME64	This is an upgrade to the electrical protocols used in VME to allow 64 bit transfers.
VME64x	VME64 Extensions. This is both an electrical and mechanical upgrade to VME64. It is forward compatible to VME64. The mechanical upgrade makes use of the 5 row VMEbus connector and also allows the use of a 5 row 2mm P0 connector.

1.4 Standard Terminology

To avoid confusion and to make very clear what the requirements for compliance are, many of the paragraphs in this standard are labeled with keywords that indicate the type of information they contain. The keywords are listed below:

- Rule
- Recommendation
- Suggestion
- Permission
- Observation

Any text not labeled with one of these keywords describes structure or operation. It is written in either a descriptive or a narrative style. These keywords are used as follows:

Rule <chapter>.<number>:

Rules form the basic framework of this draft standard. They are sometimes expressed in text form and sometimes in the form of figures, tables or drawings. All rules shall be followed to ensure compatibility between board and backplane designs. All rules use the "shall" or "shall not" words to emphasize the importance of the rule. The "shall" or "shall not" words are reserved exclusively for stating rules in this draft standard and are not used for any other purpose.

Recommendation <chapter>.<number>:

Wherever a recommendation appears, designers would be wise to take the advice given. Doing otherwise might result in some awkward problems or poor performance. While the architecture has been designed to support high-performance systems, it is possible to design a system that complies with all the rules but has abysmal performance. In many cases a designer needs a certain level of experience in order to design boards that deliver top performance. Recommendations found in this standard are based on this kind of experience and are provided to designers to speed their traversal of the learning curve. All recommendations use the "should" or "should not" words to emphasize the importance of the recommendation. The "should" or "should not" words are reserved exclusively for stating permissions in this draft standard and are not used for any other purpose.

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Suggestion <chapter>.<number>:

A suggestion contains advice which is helpful but not vital. The reader is encouraged to consider the advice before discarding it. Some design decisions that need to be made in designing boards are difficult until experience has been gained. Suggestions are included to help a designer who has not yet gained this experience. Some suggestions have to do with designing boards that can be easily reconfigured for compatibility with other boards, or with designing the board to make the job of system debugging easier.

Permission <chapter>.<number>:

In some cases a rule does not specifically prohibit a certain design approach, but the reader might be left wondering whether that approach might violate the spirit of the rule or whether it might lead to some subtle problem. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. All permissions use the "may" words to emphasize the importance of the permission. The lower-case "may" words are reserved exclusively for stating permissions in this draft standard and are not used for any other purpose.

Observation <chapter>.<number>:

Observations do not offer any specific advice. They usually follow naturally from what has just been discussed. They spell out the implications of certain rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules so that the reader understands why the rule must be followed.

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Chapter 2

Specification

2.1 Introduction

This standard is based on existing industry practices. It collects the relevant pinouts as referenced in IEEE P1386-199x CMC Draft Standard, April 4, 1995 and CMC/P1386, Draft 2.0 - Major Text Edits, October 14, 1997 into this standard.

Four patterns for mapping I/O leads from the host PMC connector to the host backplane connector are defined. Multiple mapping patterns are required because a fixed set of backplane I/O may need to be shared among several PMC positions. Many of the VME64 applications, such as telecom, military and industrial, require that I/O signals be routed from the host board through the rear backplane. Front panel I/O is not practical due to cabling problems and other environmental considerations. With the use of mezzanine cards for modular I/O, it is necessary to develop a consistent scheme for routing of these I/O signals between the mezzanine card's connector(s) and the host's rear connector.

There are four basic mappings

1. PMC to VME-P0
2. PMC to VME-P2-rows-a,c
3. PMC to VME64x-P2-rows-d,z
4. Dual PMC to 64 pins of VME-P2-rows-a,c

This standard also defines the mnemonics to use when specifying a product. The interoperability section defines recommended combinations of these mappings for use.

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2.2 Mapping of PMC-P4 to VME-P0

VME64x boards have available 95 user IO pins defined on the P0 connector. 64 of these pins can be mapped directly to PMC-P4 user IO pins. The remaining 31 can be used by the host for other functions.

Rule 2.2.1

A host that is compliant to the PMC-P4 to VME-P0 mapping shall have a pinout that complies with Table 2.2.1. An alternate view of this mapping is shown in Table 2.2.2. It is from the point of view of the P0 connector.

Rule 2.2.2

The mnemonic “P4V0-64” shall be used to signify a compliant VITA-35 PMC-P4 to VME-P0 mapping on the host as per Table 2.2.1

PMC P4	VME P0	PMC P4	VME P0	PMC P4	VME P0	PMC P4	VME P0
1	4e	2	4d	33	13c	34	13b
3	4c	4	4b	35	13a	36	14e
5	4a	6	5e	37	14d	38	14c
7	5d	8	5c	39	14b	40	14a
9	5b	10	5a	41	15e	42	15d
11	6e	12	6d	43	15c	44	15b
13	6c	14	6b	45	15a	46	16e
15	6a	16	7e	47	16d	48	16c
17	7d	18	7c	49	16b	50	16a
19	7b	20	7a	51	17e	52	17d
21	8e	22	8d	53	17c	54	17b
23	8c	24	8b	55	17a	56	18e
25	8a	26	12e	57	18d	58	18c
27	12d	28	12c	59	18b	60	18a
29	12b	30	12a	61	19e	62	19d
31	13e	32	13d	63	19c	64	19b

Table 2.2.1 : PMC-P4 mapping to VME-P0

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Pos	f	e	d	c	b	a
1	GND	--	--	--	--	--
2	GND	--	--	--	--	--
3	GND	--	--	--	--	--
4	GND	1	2	3	4	5
5	GND	6	7	8	9	10
6	GND	11	12	13	14	15
7	GND	16	17	18	19	20
8	GND	21	22	23	24	25
9	GND	--	--	--	--	--
10	GND	--	--	--	--	--
11	GND	--	--	--	--	--
12	GND	26	27	28	29	30
13	GND	31	32	33	34	35
14	GND	36	37	38	39	40
15	GND	41	42	43	44	45
16	GND	46	47	48	49	50
17	GND	51	52	53	54	55
18	GND	56	57	58	59	60
19	GND	61	62	63	64	--

Table 2.2.2 : VME-P0 mapping to PMC-P4

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2.3 Mapping of Single PMC-P4 to VME-P2-Rows-A,C

VME64 and VME64x boards have available 64 user IO pins defined on rows A and C of the P2 connector. These pins can be mapped directly to PMC-P4 user IO pins.

Rule 2.3.1

A host that is compliant to the PMC-P4 to VME-P2-Rows-A,C mapping shall have a pinout that complies to Table 2.3.

Rule 2.3.2

The mnemonic "P4V2-64ac" shall be used to signify a compliant VITA-35 PMC-P4 to VME-P2-Rows-A,C mapping on the host as per Table 2.3.

PMC P4	VME P2	PMC P4	VME P2	PMC P4	VME P2	PMC P4	VME P2
1	1C	2	1A	33	17C	34	17A
3	2C	4	2A	35	18C	36	18A
5	3C	6	3A	37	19C	38	19A
7	4C	8	4A	39	20C	40	20A
9	5C	10	5A	41	21C	42	21A
11	6C	12	6A	43	22C	44	22A
13	7C	14	7A	45	23C	46	23A
15	8C	16	8A	47	24C	48	24A
17	9C	18	9A	49	25C	50	25A
19	10C	20	10A	51	26C	52	26A
21	11C	22	11A	53	27C	54	27A
23	12C	24	12A	55	28C	56	28A
25	13C	26	13A	57	29C	58	29A
27	14C	28	14A	59	30C	60	30A
29	15C	30	15A	61	31C	62	31A
31	16C	32	16A	63	32C	64	32A

Table 2.3 : PMC-P4 mapping to VME-P2

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2.4 Mapping of Single PMC-P4 to VME64x-P2-Rows-D,Z

VME64x boards use the expanded 160 pin connectors for both the P1 and P2 connectors. These connectors provide an additional two rows of contacts, with 32 pins per row. The added rows on the P2 connector provide 46 more user defined I/O pins. The other 18 pins in the D & Z rows are pre-assigned to 17 grounds and one to a pre-charge power (VPC). These 46 user IO pins are mapped to PMC-P4 user IO pins.

Rule 2.4.1

A host that is compliant to the PMC-P4 to VME64x-P2-Rows-D,Z mapping shall have a pinout that complies with Table 2.4.1. An alternate view of this mapping is shown in Table 2.4.2. It is from the point of view of the P2 connector.

Rule 2.4.2

The mnemonic “P4V2-46dz” shall be used to signify a compliant VITA-35 PMC-P4 to VME64x-P2-Rows-D,Z mapping on the host as per Table 2.4.1.

PMC P4	VME P2	PMC P4	VME P2
1	1d	2	1z
3	2d	4	3d
5	3z	6	4d
7	5d	8	5z
9	6d	10	7d
11	7z	12	8d
13	9d	14	9z
15	10d	16	11d
17	11z	18	12d
19	13d	20	13z
21	14d	22	15d
23	15z	24	16d
25	17d	26	17z
27	18d	28	19d
29	19z	30	20d
31	21d	32	21z
33	22d	34	23d
35	23z	36	24d
37	25d	38	25z
39	26d	40	27d
41	27z	42	28d
43	29d	44	29z
45	30d	46	31z

Table 2.4.1 : PMC-P4 mapping to VME-P2

Position	VME-P2-Row d	VME-P2-Row z
1	1	2
2	3	GND
3	4	5
4	6	GND
5	7	8
6	9	GND
7	10	11
8	12	GND
9	13	14
10	15	GND
11	16	17
12	18	GND
13	19	20
14	21	GND
15	22	23
16	24	GND
17	25	26
18	27	GND
19	28	29
20	30	GND
21	31	32
22	33	GND
23	34	35
24	36	GND
25	37	38
26	39	GND
27	40	41
28	42	GND
29	43	44
30	45	GND
31	GND	46
32	VPC	GND

Table 2.4.2 : VME64x-P2 mapping to PMC-P4

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2.5 Mapping of Dual PMC-P4 to VME-P2-Rows-A,C

For a VME64 host with two PMC slots, the I/O mapping is defined in Table 2.5. In this pattern, the lower numbered 32 pins of each PMC is shared between the 64 pins of the P2 connector.

Rule 2.5.1

A host that is compliant to the Dual PMC-P4 to VME-P2-Rows-A,C mapping shall have a pinout that complies with Table 2.5.

Rule 2.5.2

The mnemonic "P4V2-32+32ac" shall be used to signify a compliant VITA-35 PMC-P4 32+32 I/O routing scheme to VME64x-P2-Rows-A,C mapping on the host as per Table 2.5.

Observation 2.5

This mapping is per reference CMC/P1386, Draft 2.0 - Major Text Edits, October 14, 1997. The 32+32 mappings as per reference IEEE P1386-199x CMC Draft Standard, April 4, 1995 is not defined here.

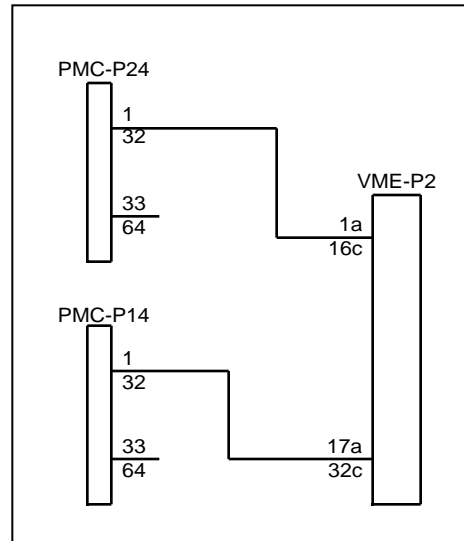


Figure 2.5 : Dual PMC Mapping

The 1995 mappings are more accurately defined as 64+32. It maps all 64 pins of P24 to VME-P2 and pins 33-64 of PMC-P14 to VME-P2 17a-32c. This mapping is not included here because it is not a universal solution. This mapping could create conflicts when two PMC modules are installed. One can still use the IEEE spec if this mapping is required.

PMC P24	VME P2	PMC P24	VME P2	PMC P14	VME P2	PMC P14	VME P2
1	1C	2	1A	1	17C	2	17A
3	2C	4	2A	3	18C	4	18A
5	3C	6	3A	5	19C	6	19A
7	4C	8	4A	7	20C	8	20A
9	5C	10	5A	9	21C	10	21A
11	6C	12	6A	11	22C	12	22A
13	7C	14	7A	13	23C	14	23A
15	8C	16	8A	15	24C	16	24A
17	9C	18	9A	17	25C	18	25A
19	10C	20	10A	19	26C	20	26A
21	11C	22	11A	21	27C	22	27A
23	12C	24	12A	23	28C	24	28A
25	13C	26	13A	25	29C	26	29A
27	14C	28	14A	27	30C	28	30A
29	15C	30	15A	29	31C	30	31A
31	16C	32	16A	31	32C	32	32A

Table 2.5 : Dual PMC-P4 mapping to VME-P2-a,c

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2.6 Interoperability

The following observation and recommendation aid in the interoperability of the mated PMC and host pair.

Observation 2.6.1

There is no specification for the electrical properties for the routings of the signals between the PMC and VME connectors. The mappings alone between PMC-P4 and VME-P0-P2 are adequate for lower speed signals. Further information is required by system designers for higher speed signals. Recommendation 2.6.1 provides the system designer with this information.

Recommendation 2.6.1

It is recommended that the host vendor publish signal routing properties. As a minimum trace lengths and impedances should be made available. Models of the connectors would also be useful.

Recommendation 2.6.2

A host supporting a single PMC with IO connections on P4 should support only one of the following configurations:

- P4V0-64
- P4V2-64ac
- P4V2-46dz

Recommendation 2.6.3

A host supporting two PMCs with IO connections on P4 should support only one of the following configuration pairs:

- P4V0-64, P4V2-64ac
- P4V0-64, P4V2-46dz
- P4V2-64ac, P4V2-46dz
- P4V2-32+32ac

Recommendation 2.6.4

Dual PMC site VME64x boards without a P0 connector could utilize some of the user-defined P2 connector pins for non-PMC IO signals. When this situation exists the non-PMC IO signals should be assigned to a consecutive number of user-defined P2 connectors pins starting from the end of either Table 2.3 or 2.4.1/2.4.2. For example, if 5 non-PMC IO signals were assigned to rows d and z of the P2 connector then user-defined pins 28d, 29d, 29z, 30d, and 31z should be utilized. Another way to view this is that PMC modules should assign their pinout usage starting from pin 1 and use the higher pins last whenever possible.

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